Manual P/N 454-44000

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User's Manual

BVME4000/6000

MC68040/68060 SINGLE BOARD COMPUTER

Board Revision F
Manual Revision I 21 February 2001

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Do not lever out any devices from the product, which uses surface-mounted devices extensively, as these can be fractured by excessive force.

This product uses devices sensitive to static electricity. Ensure adequate static electricity precautions are observed when handling the product and associated devices.

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WARNINGS

Do not lever out the EPROM's from the BVME4000/6000. The board uses surface-mounted devices extensively, which can be fractured by excessive force. Use proper EPROM extraction and insertion tools. **Damage may result if users attempt to remove or fit EPROM's incorrectly.**

Do not lever out the IP's from the BVME4000/6000. The board uses surface-mounted devices extensively, which can be fractured by excessive force. **Damage may result if users attempt to remove or fit IP's incorrectly.**

Do not lever out memory modules from the BVME4000/6000. The board uses surface-mounted devices extensively, which can be fractured by excessive force. Memory modules are not a field-fit option. **Damage may result if users attempt to remove or fit memory modules incorrectly.**

Do not fit/remove the 68040/68060 device to/from the BVME4000/6000. Special tools are required to fit and remove these devices and the correct voltage settings must be selected. Return the board to the factory if the 68040/68060 device requires changing. **Damage may result if users attempt to fit or remove the 68040/68060 device.**

The BVME4000/6000 uses devices sensitive to static electricity. Ensure adequate static electricity precautions are observed when handling the BVME4000/6000, EPROM's, IP's and memory modules.

Ensure the correct polarity of connections to the BVME4000/6000. In particular ensure the correct polarity of connections to the P2 I/O connector, incorporating the SCSI connections. **Damage may result if users fail to observe correct connection polarity to the BVME4000/6000.**

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1. Introduction

1.1 Scope

This manual provides :-

- A getting started guide.
- Configuration details.
- A user reference guide.
- A memory map.
- A map of all register locations.
- A detailed description of all dedicated registers.
- Details of implementation specific considerations for major devices.
- General hardware description.

This manual does not provide:-

- Detailed data on the operation of the major devices.
- Details of VMEbus & IndustryPack™ Specifications.

Information is provided to allow the module to be integrated into a system and configured by the system software. This User Manual is intended for use by system integrators, service personnel, software engineers and end users.

Unless otherwise stated, address information is in hexadecimal notation.

The term "IP" is used as an abbreviation for "IndustryPack™" throughout this manual.

1.2 BVME4000 Part Numbers

452-40231/40331	MC68EC040	25/33MHz, VMEbus I/F, ETHERNET, SCSI, IP I/F, 2Mb SRAM
452-42231/42331	MC68040	25/33MHz, VMEbus I/F, ETHERNET, SCSI, IP I/F, 2Mb SRAM

Other versions of the BVME4000 are available to special order, where any of the VMEbus I/F, ETHERNET, SCSI & IP I/F may be omitted or 512Kb SRAM fitted. Contact your supplier for details.

1.3 BVME6000 Part Numbers

452-40631	MC68EC060	66MHz, VMEbus I/F, ETHERNET, SCSI, IP I/F, 2Mb SRAM
452-42531	MC68060	50MHz, VMEbus I/F, ETHERNET, SCSI, IP I/F, 2Mb SRAM

Other versions of the BVME6000 are available to special order, where any of the VMEbus I/F, ETHERNET, SCSI & IP I/F may be omitted or 512Kb SRAM fitted. Contact your supplier for details.

1.4 Memory Module Part Numbers

453-82390/83390	MEM390 25(50)/33(66)MHz	4Mbyte DRAM *
453-82403/83403	MEM400 25(50)/33(66)MHz	16Mbyte DRAM & 4Mbyte FLASH
453-82404/83404	MEM400 25(50)/33(66)MHz	16Mbyte DRAM & 8Mbyte FLASH
453-82482/83482	MEM480 25(50)/33(66)MHz	48Mbyte DRAM *
453-85016/86016	MEM4SD 25(50)/33(66)MHz	16Mbyte SDRAM
453-87064/88064	MEM4SD 25(50)/33(66)MHz	64Mbyte SDRAM
453-87128/88128	MEM4SD 25(50)/33(66)MHz	128Mbyte SDRAM
453-89256/90256	MEM4SD 25(50)/33(66)MHz	256Mbyte SDRAM

Other Memory Module types and options are available, * denotes type not recommended for new designs. Some Memory Module types can also be "stacked" two high, to increase capacity or mix memory types. Contact your supplier for details.

2. Overview

2.1 Board Layout

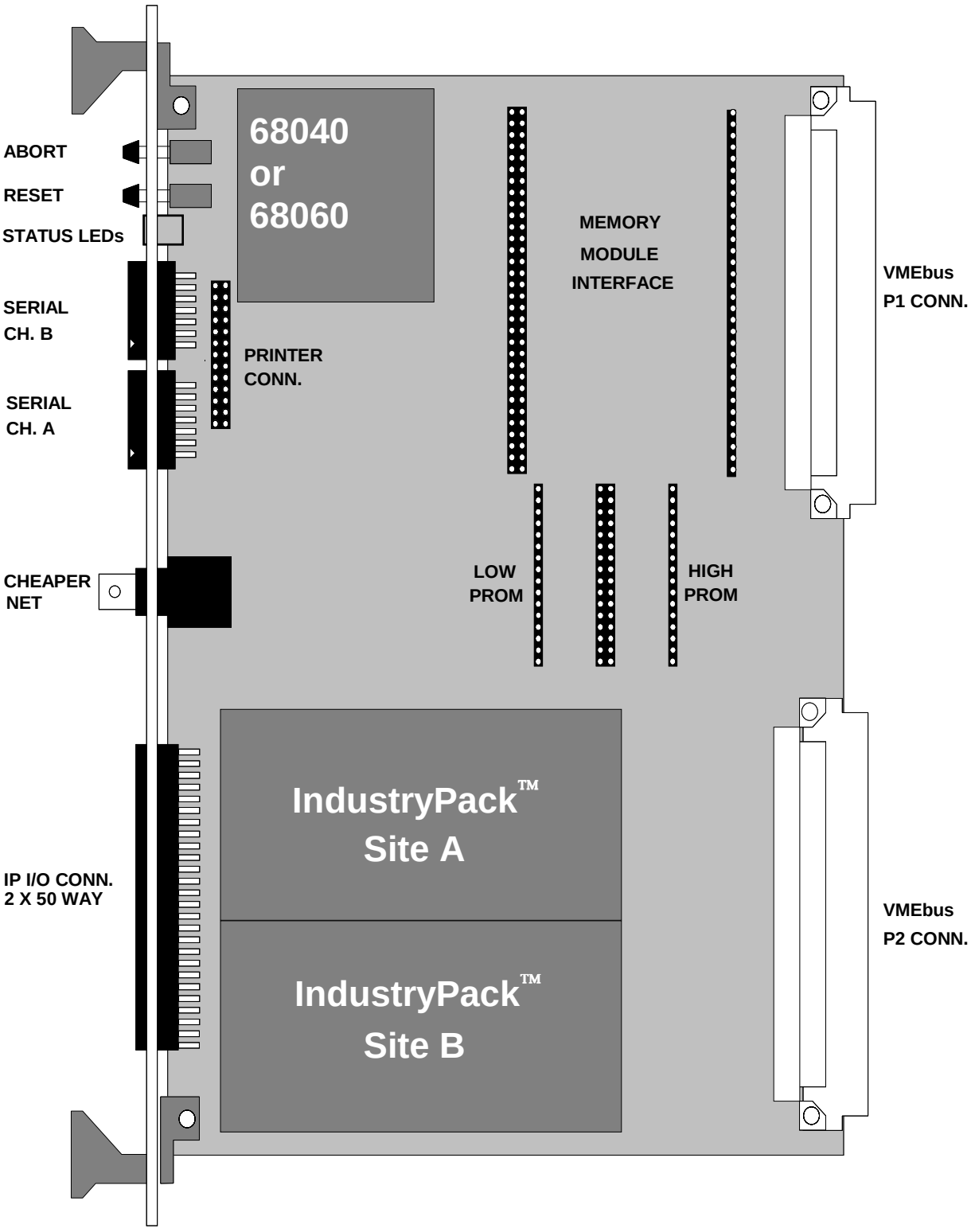


Figure 1 Board Layout

2.2 Features

- BVME4000 - MC68040 CPU (MC68EC040/68LC040 options).
  - ❍ 25 MHz and 33 MHz clock speed variants.
  - ❍ 4096 byte data and instruction caches.
- BVME6000 - MC68060 CPU (MC68EC060/68LC060 options).
  - ❍ 50 MHz and 66 MHz clock speed variants (25 MHz or 33 MHz bus).
  - ❍ 8192 byte data and instruction caches.
- 32-bit wide burst fill Dual Ported (with Bus Snooping) memory module interface with NO capacity limitations allowing many options, for example:
  - ❍ 8Mbytes of FLASH EPROM (Erasable, Programmable non-volatile storage).
  - ❍ 256Mbytes DRAM.
- 2Mbyte EPROM pair (16-bit wide), supports 5V FLASH (1Mbyte).
- 512K/2Mbyte Non-volatile (battery backed) SRAM (32-bit wide).
- 2Kbit EEPROM (NMC24C02).
- High Performance DMA driven 5Mbyte/sec SCSI Interface (NCR53C710).
- High Performance DMA driven Ethernet/Cheapernet (10BaseT option) (82596CA).
- Two 16-bit IP Compatible Sites (Double height 32-bit access supported).
  - ❍ Expansion Connector allowing 4 IP Compatible Site daughter board.
  - ❍ 8MHz, 32MHz and proprietary high speed 'Source Synchronous Modes' supported.
- Two Interrupt driven serial I/O ports - RS232, RS422 and RS485 options (Z85230).
- Real Time Clock (Battery backed) Including Tick timer, 2 16-bit timers and non-volatile configuration RAM (DP8570).
- Bi-directional Parallel port including one further 24-bit interrupting Counter/timer (MC68230).
- Optimised A32,A24,A16:D32,D16,D08 master/slave VMEbus interface.
  - ❍ VMEbus Interrupter.
  - ❍ VMEbus Interrupt handler.
  - ❍ Location monitor - Mailbox Interrupts.
- VMEbus System Controller Functions.
  - ❍ Four level Arbiter (programmable ROR, RWD and SGL).
  - ❍ RESET, SYSCLK generator.
- Single slot, 6U form factor.
- Available built as a single solution disc based module.
- OS-9, VxWorks, Linux & debug monitor software support.
- Fully compatible to VMEbus specification revision C.1.

2.3 Applications

- VMEbus Main System Processor.
- VMEbus Intelligent I/O Processor.
- High Performance Embedded Processor.

3. Description

3.1 Block Diagram

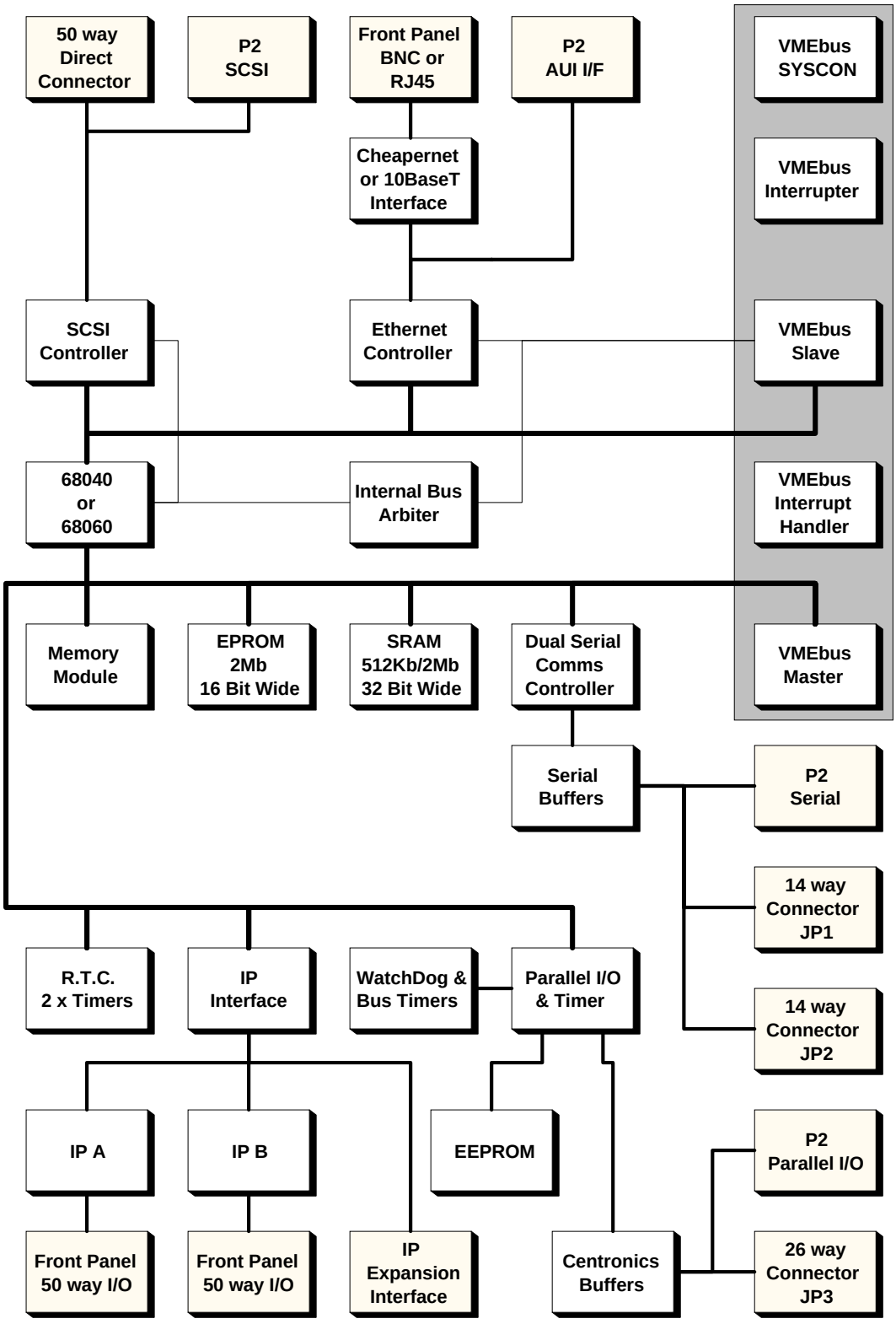


Figure 2 Block Diagram

3.2 Processor

The BVME4000 is based on the MC68040 32-bit processor from Motorola running at 25 or 33MHz. This virtual memory processor provides a MC68030 compatible integer processor running concurrently with an IEEE754 compatible floating-point unit (FPU). In addition two fully independent data and instruction demand page memory management units (MMU's) and two independent 4Kbyte caches provide efficient bus interface with a high degree of instruction execution parallelism.

The BVME6000 is similar to the BVME4000, but is based on the MC68060 32-bit processor from Motorola running at 50MHz with a 25MHz bus. The MC68060 provides a MC68040 compatible integer processor running concurrently with a MC68040 IEEE754 compatible floating-point unit (FPU). In addition two fully independent data and instruction MC68040 compatible demand page memory management units (MMU's) and two independent 8Kbyte caches.

The BVME4000 and BVME6000 are also available in lower cost versions with the MC68LC040/68LC060, which provide the same functionality as the MC68040/68060, but without the FPU, and with the MC68EC040/68EC060 which provide the same functionality, but without the MMU or FPU. The MC68LC060/68EC060 can run at 50 or 66MHz with a 25 or 33MHz bus respectively.

3.3 Memory

The BVME4000/6000 may be fitted with a large variety of 32-bit wide, burst fill memory devices. The BVME4000/6000 uses the BVM memory module interface which provides a full 32-bit MC68040/68060 bus, and supports 2/1/1/1 (no wait state) accesses to a variety of standard BVM memory modules, allowing use of memory modules which currently include:

- 8 to 48Mbytes DRAM (5/3/3/3 access at 33MHz bus clock).
- 16 to 512Mbytes DRAM (4/1/1/1 read, 3/2/2/2 write at 25 & 33MHz bus clock).
- 16Mbytes DRAM plus 8Mbyte FLASH EPROM (4/2/2/2 DRAM, 5/2/2/2 FLASH access).

This memory can be dual ported allowing concurrent accesses by both the processor and other VMEbus masters. These accesses may be 'snooped' by the processor to maintain cache coherency. This, together with the onboard 'location monitor' allows full multiprocessor communication with other CPU (and DMA) VMEbus cards.

The BVME4000/6000 also provides 2Mbytes (512Kbytes to special order) of battery-backed 32-bit wide Static RAM, providing a 5 CPU clock cycle access at 25MHz or 33MHz bus clock. This SRAM may be used for non-volatile storage applications, or as main system memory in applications where a memory module is not fitted. The SRAM can also be dual ported to the VMEbus.

A pair of 32-pin JEDEC pinout sockets provide up to 2Mbytes of 16-bit wide EPROM providing a 10 CPU clock cycle access at 25MHz or 33MHz bus clock. These sockets can support 512K, 1M, 2M, 4M and 8Mbit EPROM devices, and up to 4Mbit 5V FLASH devices.

3.4 Real Time Clock

The BVME4000/6000 provides a battery backed Real Time Clock using the DP8570 device. This device is battery backed, and maintains date and time data. The DP8570 can also generate an interrupt from it's periodic timer from 1mS to 1 second, or from two other independent 16-bit timers on chip. The timers offer a resolution of up to 500nS, and can be used in one-shot or periodic interrupt mode. A small amount of non-volatile storage is also provided for system configuration purposes. The DP8570 is battery backed using a lithium battery giving typically 10 years of non-volatile operation.

3.5 Serial Communications

Two serial communications interfaces are provided from a Z85230 SCC device. The Z85230 provides both synchronous (SDLC/HDLC) and asynchronous protocols. Asynchronous baud rates of up to 115.2Kbit/s (using the on-board crystal) are supported. Field changeable buffer modules allow RS232, RS422 or RS485 electrical interfaces to be selected for either (or both) channels. The two serial interfaces are available on the front panel, or via the rear P2 connector. The synchronous clock signals are also available via the P2 connector.

3.6 Parallel Port

An 8-bit, bi-directional I/O port with interrupt driven handshake is provided allowing direct connection to Centronics devices. This is implemented in a 68230 which includes a further 24-bit timer with interrupt capability. This device also provides part of the board control functions, and is used to control the software watchdog function. The parallel port is connected to a dedicated connector near the front panel, or via the P2 connector.

3.7 SCSI Interface

A SCSI interface is provided built around the NCR53C710. This provides asynchronous transfers of up to 5Mbytes per second. The 32-bit DMA driven interface allows direct access to the entire memory map of the BVME4000/6000. The burst mode interface stacks up 16 bytes at a time and transfers them as a line transfer at up to 4/2/2/2 access speeds at 25MHz bus clock. At 5Mbyte/s this gives a 400nS burst every 3.2µS or 12.5% bus bandwidth requirement. The 53C710 is an intelligent processor in its own right, running SCSI SCRIPTS software. This enables very high level commands to be issued to the SCSI interface further minimising processor overhead. The SCSI interface is connected to a dedicated 50-way connector and is also available via the P2 connector.

3.8 Ethernet Interface

An Ethernet Interface is provided built around the Intel 82596CA. This provides a 32-bit DMA driven interface to both Ethernet (via the AUI interface on the P2 connector) and either Cheapernet (via a front panel BNC) or optionally 10BaseT (via a front panel RJ45). The 32-bit DMA driven interface allows direct access to the entire memory map of the BVME4000/6000 allowing full packet management by the 82596CA. Each 32-bit transfer requires 320nS maximum (including arbitration) to execute the cycle. A transfer will occur no more frequently than every 4µS (4 bytes at 1Mbyte per second). Thus worst case bus bandwidth requirement is 8% at 25MHz bus clock.

3.9 IP I/O

Two standard IP compatible sites are provided. The IP interface complies fully with the IP specification. The two sites may be used individually for single IP's which are accessed as 16-bit wide, or as a pair for double IP's, which are accessed as 32-bit wide. IP operation is supported at 8MHz, 32MHz, and CPU synchronous speeds. The IP DMA function is not supported by these two sites, but may be supported on an IP daughter board (see below). The IP ID and I/O spaces are 256bytes each, and the memory spaces are 8Mbytes. IP vectored interrupts are fully supported and the interrupt levels may be individually programmed.

An IP expansion bus connector is provided to allow additional IP's to be supported. A further 4 IP's may be added on a daughter board connected to this expansion interface. Two 'virtual IP' sites are also available for controlling the daughter board IP interface. The daughter board may include a local DMA controller and RAM which is accessed through one of the 'virtual IP' sites, thus supporting the IP DMA function.

3.10 VMEbus Interface

Full VMEbus system controller functions are provided including SYSCLK drive, Bus time out monitor, SYSRESET drive and an efficient 4 level bus arbiter working in prioritised (PRI), single level (SGL), or round robin (RRS) arbitration modes.

3.10.1 VMEbus Master

Byte or Word Master accesses may be made to the Standard (A24) and Short I/O (A16) address spaces, Byte, Word and Longword Master accesses may be made to the Extended (A32) address space. BVME4000/6000 Longword accesses to the A24 or A16 address space may be converted to two Word cycles, or proceed as a Longword cycle dependant upon the BVME4000/6000 address space accessed. Read Modify Write (RMW) cycles are supported for all of these accesses.

VMEbus arbitration is normally configured to be Release On Request (ROR) method. This may be changed to Release When Done (RWD) with a PLD change. Both schemes use FAIR requesting, ensuring each master has an equal chance of obtaining the bus. Digital bus busy filtering and arbitration interleaving is used to ensure premium arbitration performance.

3.10.2 VMEbus Slave

The memory module and on-board SRAM are dual ported onto the VMEbus. The VMEbus base address, size of window and local base address are programmable for the A24 and A32 address spaces. The BVME4000/6000 responds to Byte and Word and Longword Slave accesses to the A32, A24 and A16 address spaces.

The BVME4000/6000 can snoop VMEbus slave accesses if enabled to do so. Thus although the CPU uses extensive caching, full coherency is maintained by the CPU providing any data that is 'stale' in the accessed memory - refer to "Appendix B CPU Cache Coherency and Bus Snooping (on page 62)".

A VMEbus location monitor is also supported in the A16 address space. This is a fixed 256byte window size, and the VMEbus base address is programmable. A local interrupt can be enabled when the A16 VMEbus window is accessed.

The BVME4000/6000 is compatible with VMEbus address pipelining and RMW cycles.

3.11 Interrupts

3.11.1 VMEbus Interrupt Handler

The BVME4000/6000 may be configured to respond to VMEbus interrupts on any of the 7 VMEbus interrupt levels. Each interrupt level may be programmed to be enabled or disabled individually.

A User vectored VMEbus interrupt causes the CPU to reply with a VMEbus Master interrupt acknowledge cycle. This cycle uses only the that is broadcast in a similar way to the addresses. The A1,2,3 address lines indicate the address level being handled.

The interrupting device returns an ID vector on the odd data byte. This is used as the user vector by the CPU.

3.11.2 Internal Interrupts

Internal CPU interrupts are generated from a variety of sources, as detailed in the table below:

Source	Level	Type
VMEIRQ7:1	IRQ7:1	Vectored
ACFAIL	7	Auto
ABORT	7	Auto
8570 RTC	6	Auto
68230 TIMER	5	Vectored
MEMORY MODULE	4	Auto
85230 SCC	3	Vectored
53C710 SCSI	3	Auto
68230 PARALLEL	2	Vectored
82596CA ETHERNET	2	Auto
LOCATION MONITOR	1	Auto
IPA, IPB INT0 & INT1	Programmable	Vectored
IP EXPANSION I/F	Programmable	Vectored

3.11.3 VMEbus Interrupter

The BVME4000/6000 may generate VMEbus interrupts on any programmable single level 1-7 and responds with a software programmable ID to the subsequent interrupt acknowledge cycle. Writing the ID to the a vector register causes a VMEbus interrupt to be generated on the selected level. The BVME4000/6000 VMEbus interrupt ID vector may be programmed to suit the application.

3.12 VMEbus System Controller Functions

The BVME4000/6000 provides a number of system controller functions that may be enabled by programming the relevant registers, or by link selection.

RESET

Asserted if +5V falls below 4.65V and when a link is installed. VMEbus RESET has a minimum asserted period of 200mS.

ARBITRATION

The BVME4000/6000 can be programmed/link selected to provide SGL, PRI or RRS arbitration.

SYSCLK

The BVME4000/6000 can be programmed/link selected to provide a 16MHz VMEbus SYSCLK.

BUS TIMER

The BVME4000/6000 can be programmed/link selected to provide a 128µS Bus Timeout BERR signal.

3.13 Power Supply Monitor/Watchdog

A MAX791 provides power up/power down control for the battery switching for the non-volatile RAM and processor RESET. It also provides a processor watchdog capability controlled via the Board Control Register. If enabled, the processor will be reset if the software fails to maintain pulses to the watchdog circuit.

3.14 Local Bus Monitor

All bus cycles (including VMEbus arbitration requests) are timed by an on-board timer. If any cycle takes longer than 64 CPU clock cycles a Transfer Error Abort signal and bus error exception vector are generated. Thus the processor cannot simply hang-up as a result of invalid addresses being generated from software. The exception to this is for VMEbus accesses - these are timed by the VMEbus Timeout monitor.

3.15 Configuration Switch

A 4-bit configuration switch is provided for software bootstrap detection. This switch does not affect the hardware directly, but is normally used by the software to set up the BVME4000/6000's configuration registers.

3.16 EEPROM

An NM24C02 serial I^2C EEPROM device provides 2Kbits of EEPROM storage for configuration settings. The NMC24C02 is accessed on the I^2C serial bus via the Board Control Register.

4. Installation

The BVME4000/6000 module is inserted into a vacant VMEbus slot. If it is to function as the system controller, then it should be positioned in slot 1. It passes through all VMEbus daisy chained arbitration signals.

IACK should be jumpered to IAKIN on the backplane at slot 1. All interrupt IAKIN to IAKOUT and BGIN to BGOUT signals should be jumpered across vacant slots to the right of the module.

If it is not the system controller, it may be located in any of the VMEbus slots to the right of the VMEbus system controller.

To install the BVME4000/6000:

1. Ensure all backplane jumpers associated with the slot for the BVME4000/6000 are removed.

2. Ensure the BVME4000/6000 module is correctly configured for the target system.

3. If the Parallel interface is to be used, plug in the parallel cable to JP3 (if not using the P2 connections).

4. Connect the SCSI cable to the 50 way SCSI connector on the BVME4000/6000 (if not using the P2 connections), ensure the correct polarity.

5. Insert the BVME4000/6000 module into the rack pushing the VMEbus connector fully home.

6. Secure the BVME4000/6000 into the rack with the two fixing screws top and bottom.

7. Plug in serial cables to JP1 and/or JP2 (if not using the P2 connections).

8. If using Cheapernet, connect the Cheapernet BNC-T connector to the BVME4000/6000 BNC connector or if using the optional 10BaseT, connect the RJ45 connector to the BVME4000/6000 RJ45 connector.

9. Connect the IP I/O connections to the two 50 way front panel connectors.

10. Ensure that the configuration switch is set up correctly for the software installation.

11. Ensure the correct application EPROM's are fitted.

Removal is the reverse of assembly.

If the test or application software fails, ensure that all installation instructions have been correctly carried out. Some typical reasons for incorrect operation are:-

1. Socketed components may become disturbed in transit. Push home all socketed components where suspect.

2. The BVME4000/6000 module uses the VMEbus Address modifier codes to determine address significance. Ensure the host CPU module produces the correct address modifier codes.

3. Ensure that all links are configured to the default set-up or that any alterations to the default are correctly configured.

4. Ensure that the VMEbus backplane (if used) is correctly configured with regard to the daisy-chain signal jumpers and the IACK termination jumpers (if any).

The BVME4000/6000 CPU requires adequate airflow across it to ensure correct operation. A heatsink may need to be fitted to the CPU - refer to "Appendix E Thermal Management (on page 68)" for more details.

5. Configuration

5.1 PCB Layout

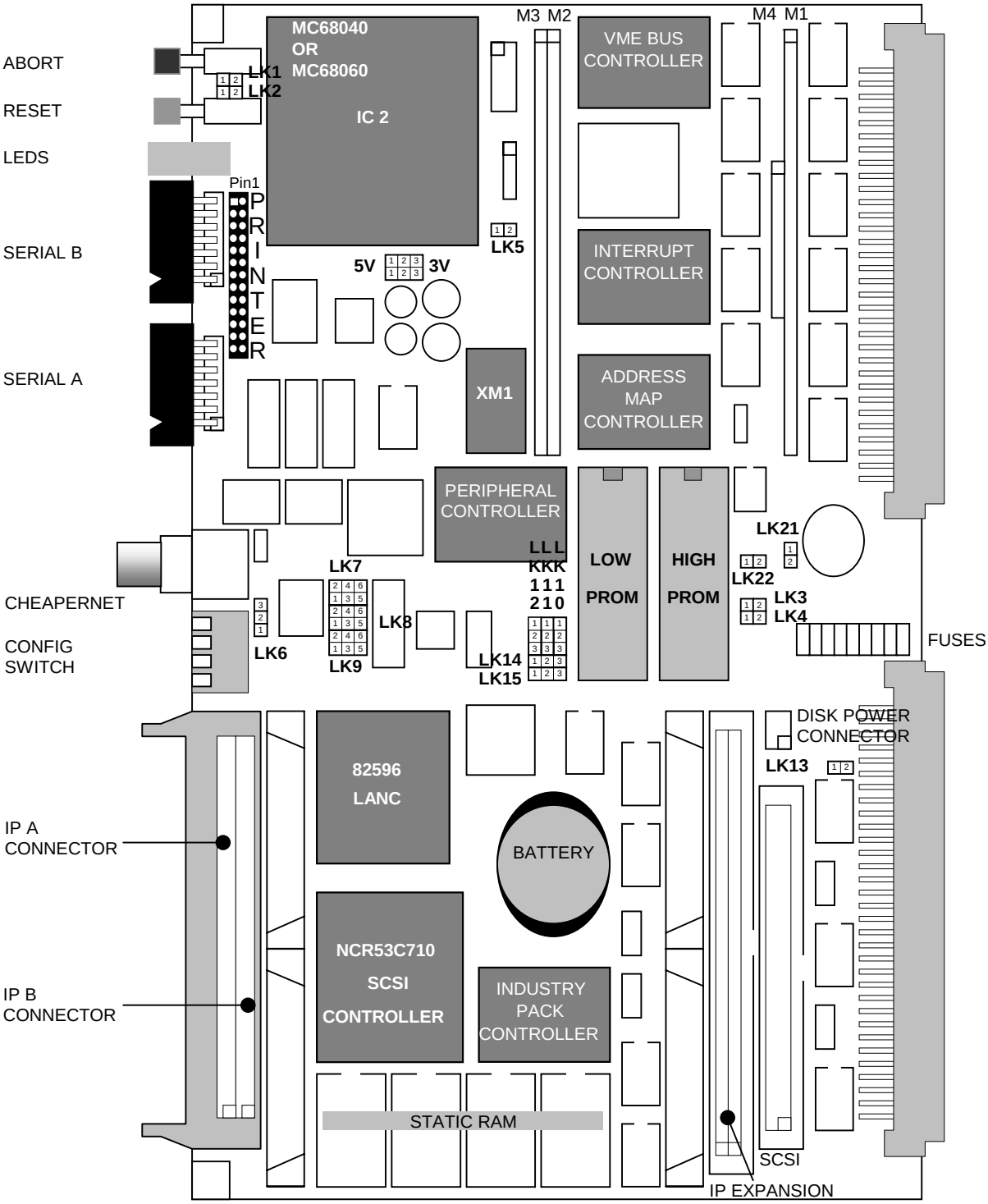


Figure 3 PCB Layout

5.2 Link and Switch Definitions

The following link definitions show the links grouped in the same orientation as the layout drawing on the previous page, i.e. with the VMEbus connectors to the right. Link positions marked with a ✪ show the default configuration.

Some of the link numbers are not described here, these are for factory use only when configuring different build variants of the BVME4000/6000 and are not available for user's.

5.2.1 LK1 Abort Switch Enable

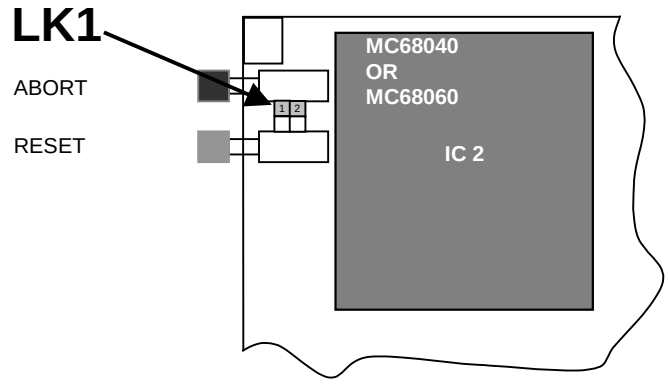


Figure 4 LK1 Abort Switch Enable Location

Fitting this link enables the ABORT switch to generate interrupts.

LK1	Function
1 & 2 Fitted ✪	ABORT Switch generates Level 7 Auto-vectored IRQ
1 & 2 Omitted	NO IRQ generated from switch

5.2.2 LK2 Reset Switch Enable

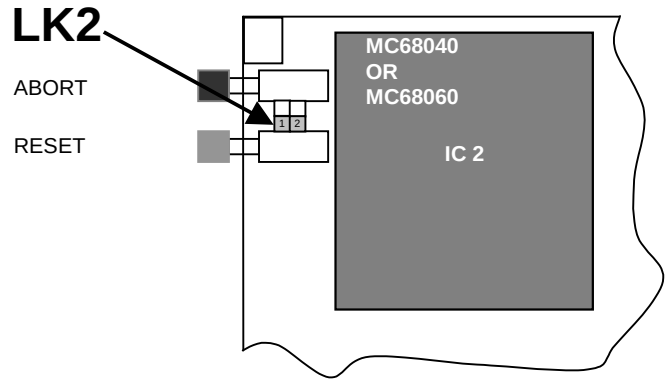


Figure 5 LK2 Reset Switch Enable Location

Fitting this link enables the RESET switch to generate a local reset and (optionally) a VMEbus RESET.

LK2	Function
1 & 2 Fitted ✪	RESET switch resets BVME4000/6000 (and VMEbus)
1 & 2 Omitted	NO RESET generated from switch

5.2.3 LK3 VMEbus Reset Out Enable

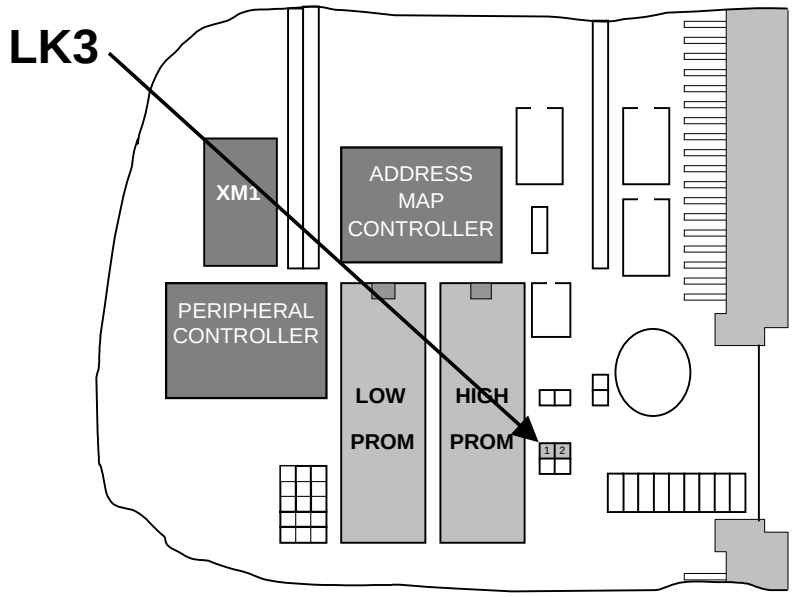


Figure 6 LK3 VMEbus Reset Out Enable Location

This link enables the VMEbus RESET to be driven by the BVME4000/6000 RESET signal.

LK3	Function
1 & 2 Fitted ✪	BVME4000/6000 RESET resets VMEbus
1 & 2 Omitted	NO VMEbus RESET from BVME4000/6000

5.2.4 LK4 VMEbus Reset In Enable

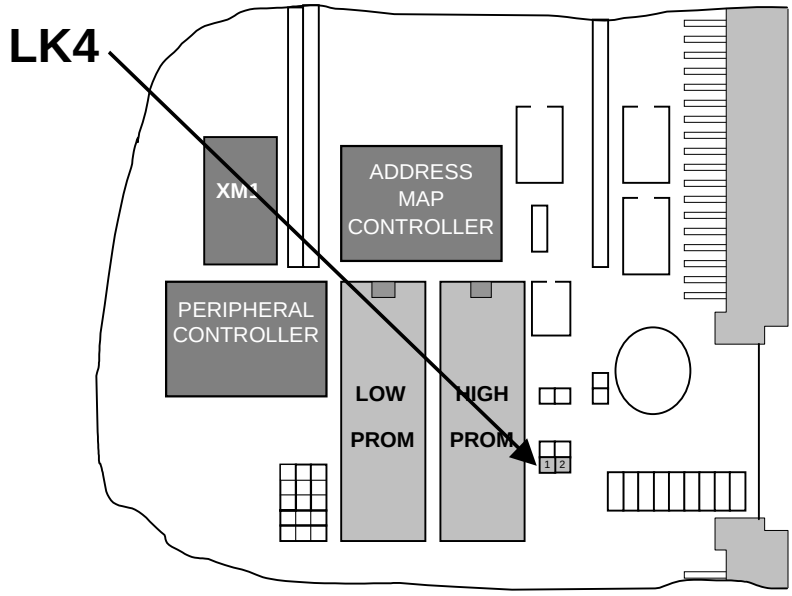


Figure 7 LK4 VMEbus Reset In Enable Location

This link allows the BVME4000/6000 to be reset from the VMEbus RESET signal.

LK4	Function
1 & 2 Fitted ✪	VMEbus RESET resets BVME4000/6000
1 & 2 Omitted	NO BVME4000/6000 RESET generated from VMEbus

5.2.5 LK5 CPU Cache Inhibit

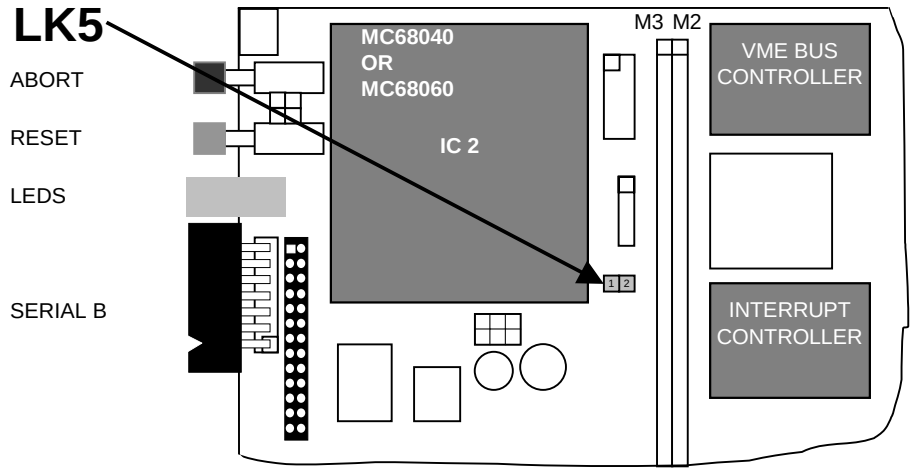


Figure 8 LK5 CPU Cache Inhibit Location

This link disables the MC68040/68060's on chip data and instruction caches to allow (for example) emulators to be used with the BVME4000/6000.

LK5	Function
1 & 2 Fitted	MC68040/68060 CACHES DISABLED
1 & 2 Omitted ✪	MC68040/68060 CACHES ENABLED

5.2.6 LK6 Cheapernet Heart Beat Enable

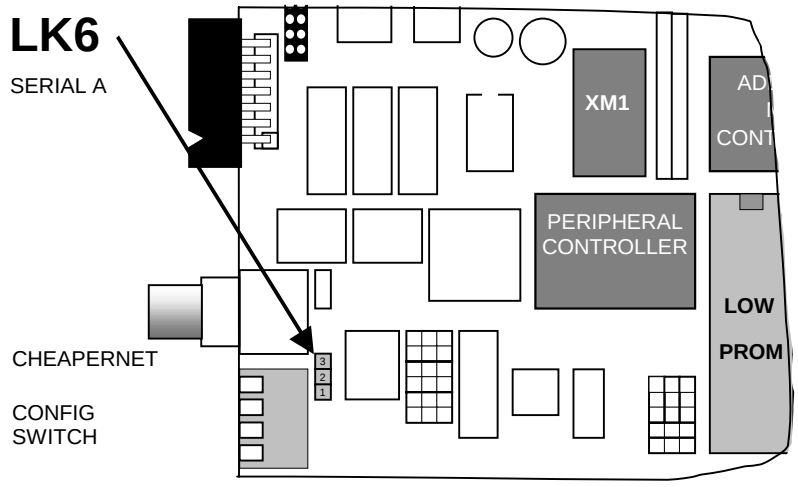


Figure 9 LK6 Cheapernet Heart Beat Enable Location

This link allows the CHEAPERNET Heartbeat function to be enabled.

LK6	Function
1 & 2 ✪	Normal operation - Heartbeat Disabled
2 & 3	Heartbeat Enabled

Note: this link is not fitted for the optional 10BaseT operation.

5.2.7 LK7,8,9 Ethernet AUI/Cheapernet Select

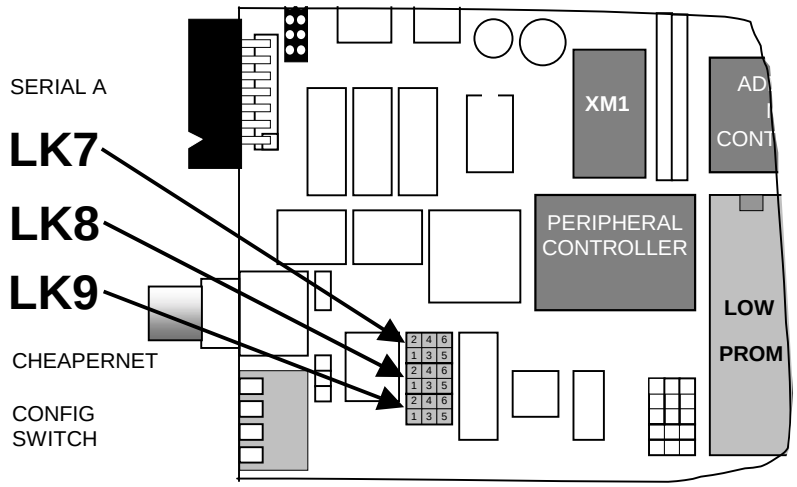


Figure 10 LK7,8,9 Ethernet AUI/Cheapernet Select Location

These links allow selection between CHEAPERNET (via front panel BNC connector) and ETHERNET AUI (via P2 connector). They must all be set in conjunction.

LK7,8,9	Function
1 & 3, 2 & 4 ✪	CHEAPERNET via front panel BNC
3 & 5, 4 & 6	ETHERNET AUI via P2 connector

Note: these links are not fitted for the optional 10BaseT operation as it is permanently selected.

5.2.8 LK10,11,12,14,15 EPROM Size & Type Select

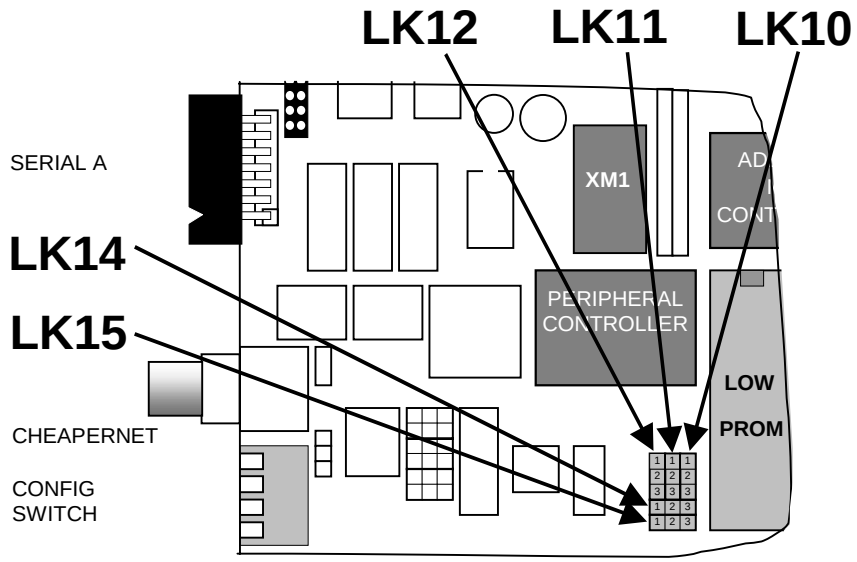


Figure 11 LK10,11,12,14,15 EPROM Size & Type Select Location

These links selects the size of EPROM in the IC44/45 32-pin EPROM sockets. A 27C512 (28-pin) EPROM should be fitted to the lower 28-pins of the socket (pins 1, 2, 31 & 32 unused).

LK10	LK11	LK12	LK14	LK15	Function
1 & 2	1 & 2	1 & 2	1 & 2	1 & 2	27C512 (512Kbit) or 27C010 (1Mbit) devices
2 & 3	1 & 2	1 & 2	1 & 2	1 & 2	27C020 (2Mbit) devices
2 & 3	2 & 3	1 & 2	1 & 2	1 & 2	27C040 (4Mbit) devices
2 & 3	2 & 3	2 & 3	1 & 2	1 & 2	27C080 (8Mbit) devices
2 & 3	2 & 3	2 & 3	2 & 3	2 & 3	AM29F010 / 020 / 040 Write Enable
2 & 3	1 & 2	2 & 3	2 & 3	2 & 3	AM29F010 / 020 / 040 Write Protect

5.2.9 LK13 SCSI Termination Disable

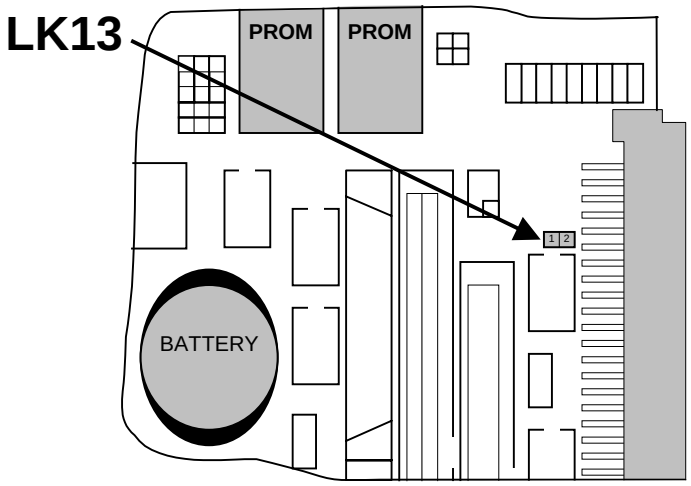


Figure 12 LK13 SCSI Termination Disable Location

This link allows the SCSI bus terminators to be enabled on the BVME4000/6000. This is necessary if the BVME4000/6000 is at the end of the SCSI bus cable, otherwise the terminators should be disabled.

LK13	Function
1 & 2 Omitted ✪	SCSI bus terminated on BVME4000/6000
1 & 2 Fitted	NO SCSI bus termination on BVME4000/6000

5.2.10 LK18,19 CPU 5/3.3V Selection

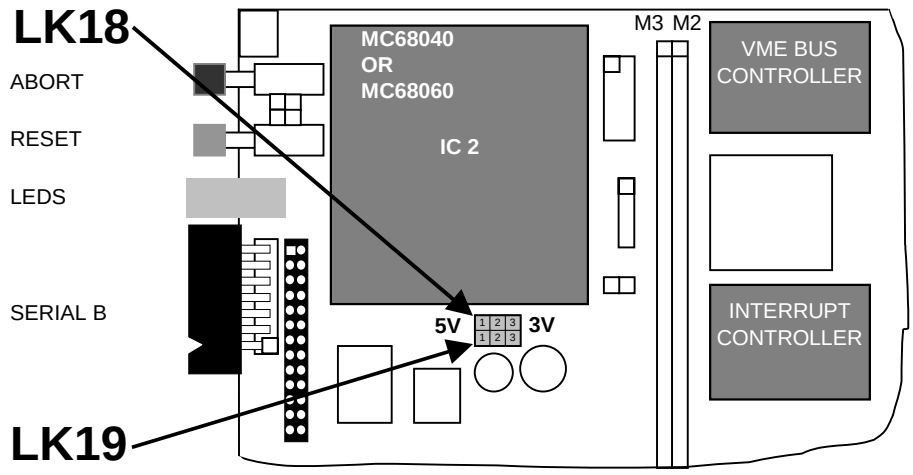


Figure 13 LK18,19 CPU 5/3.3V Selection Location

These are factory set links – when a 68040 series CPU is fitted, 5V is selected, when a 68060 series CPU is fitted 3.3V is selected. They must all be set in conjunction.

Setting these links incorrectly will cause damage to the CPU device.

LK18,19 (5V/3V)	Function
1 & 2	5 VOLTS SELECTED FOR 68040 SERIES
2 & 3	3.3 VOLTS SELECTED FOR 68060 SERIES

5.2.11 LK21 SRAM Backup Selection

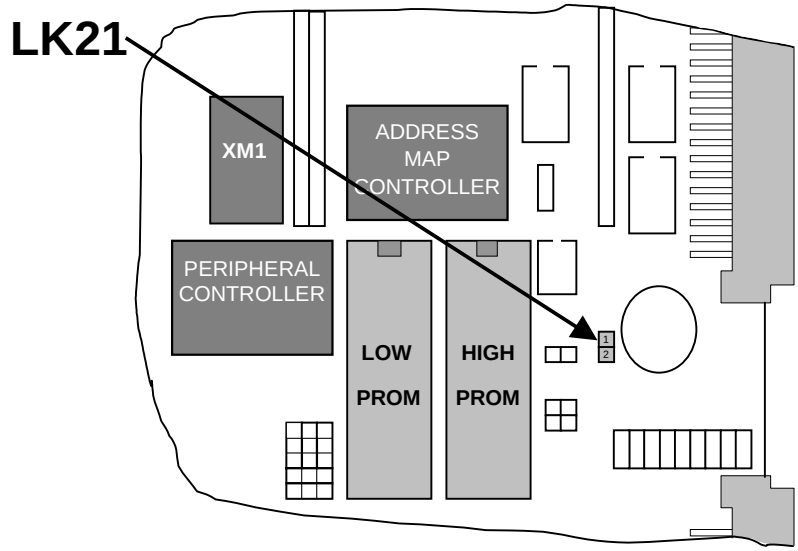


Figure 14 LK21 SRAM Backup Selection Location

This link enables the SRAM to be backed up by the on-board battery. The SRAM is always backed up by the 0.1F Memory Capacitor and the VMEbus STDBY supply.

LK21	Function
1 & 2 Fitted	SRAM is backed up by battery or MEMCAP/VMEbus STDBY
1 & 2 Omitted ✪	SRAM is only backed up by MEMCAP/VMEbus STDBY

5.2.12 LK22 VMEbus System Controller Enable

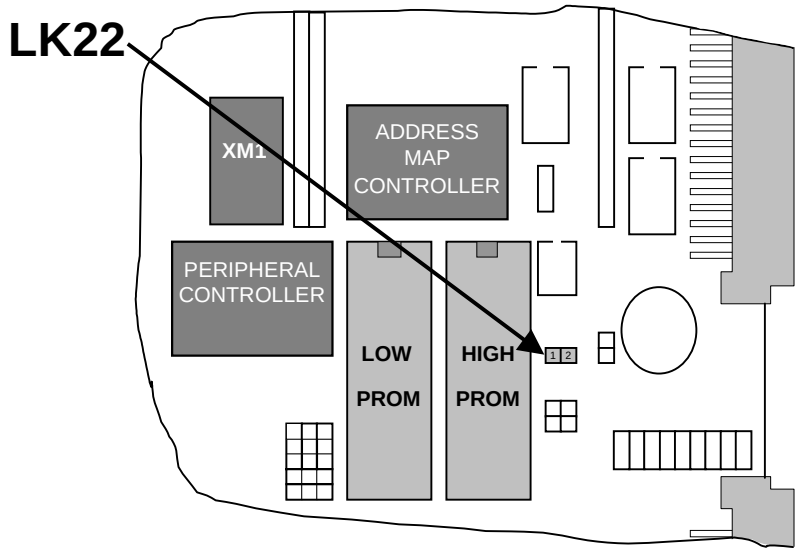


Figure 15 LK22 VMEbus System Controller Enable Location

This link forces the BVME4000/6000 to be the VMEbus System Controller, so the BVME4000/6000 performs as the VMEbus arbiter, drives VMEbus SYSCLK and VMEbus BCLR. The normal selection for this function is in the Board Control Register when not overridden by this link - refer to "7.13.3 Port B Usage (on page 52)". Omitting this link is typically required to ensure that the VMEbus SYSCLK signal is driven as the VMEbus RESET signal is de-asserted.

LK22	Function
1 & 2 Omitted	BVME4000/6000 VMEbus System Controller ENABLED
1 & 2 Fitted ✪	BVME4000/6000 VMEbus System Controller set in BCR

5.2.13 Configuration Switch

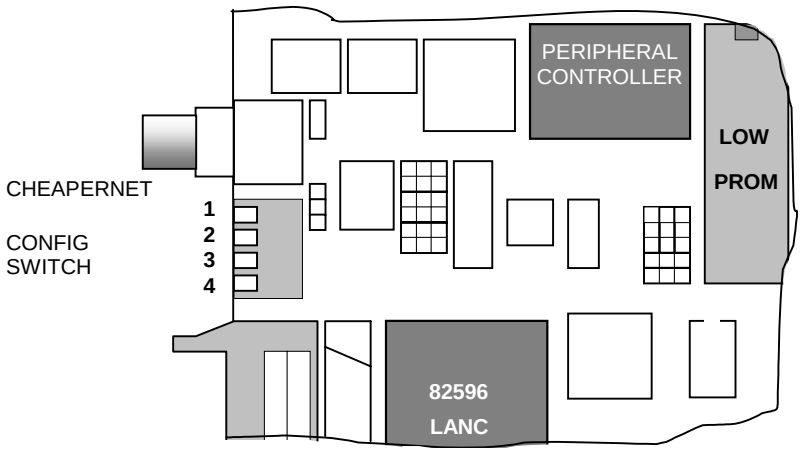


Figure 16 Configuration Switch Location

This switch can be read by software to indicate system configuration options to the boot strap routines. A switch ON selects a logical 0 for a bit and a switch OFF selects a logical 1 for a bit. Switch pole 1 relates to Bit 3, switch pole 2 to Bit 2, switch pole 3 to Bit 1, and switch pole 4 to Bit 0 in the BVME4000/6000 Configuration Switch Register - refer to "7.11.2 Configuration Switch Register (on page 49)".

5.3 Indicators

5.3.1 Green LED - RUNNING

The GREEN RUNNING LED indicates that the BVME4000/6000 is running valid code. When extinguished, the processor is either halted or stopped. The LED will also dim when the processor is executing an RTE instruction, stacking an exception frame or doing an MMU table search.

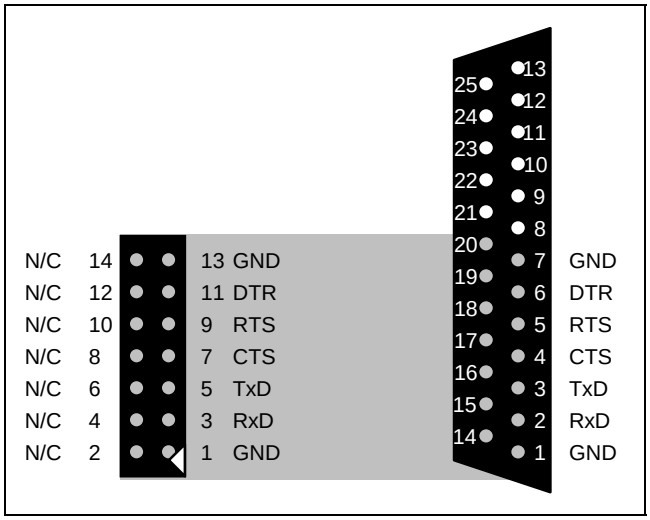
5.3.2 Red LED - VMEbus Master Access

The RED MASTER LED indicates that the BVME4000/6000 is currently an active VMEbus master.

6. Connector Pinouts

6.1 JP1 & JP2 Serial Port Connections

JP1 and JP2 carry the serial port signals for Serial Channel A and Serial Channel B respectively. JP1 (Serial Channel A) is the lower connector. The layout is designed to connect directly to a standard 25-way connector as shown:



The pinout numbering conventions are different for the two styles of connector (see diagram). However, the pinout is arranged to give a one to one connection to a 25-way D-type connector when using Insulation Displacement Connectors (IDC) and ribbon cable.

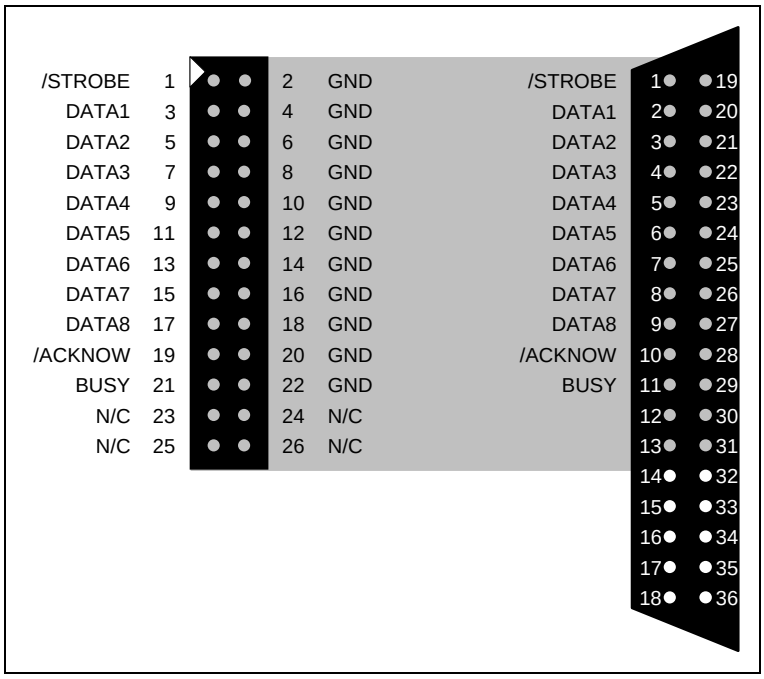
Not all the RS232 signals defined for a 25 way connector are supported by the BVME4000/6000. The cable assembly should be built such that pin 1 on the 14 way connector connects to pin 1 of the 25 way. A 14 way ribbon cable is used leaving pins 8 - 13 and 21 - 25 unconnected.

Figure 17 JP1 & JP2 Serial Port Connections

The above assumes standard RS232 drivers are fitted to the BVME4000/6000. If RS422 or RS485 interface modules are fitted refer to the RS422/RS485 INTERFACE MODULE documentation detailed in the "A.9 RS422/485 Interface Module (on page 60)" section of this manual .

6.2 JP3 Parallel Port Connections

JP3 carries the parallel port signals, and the layout is designed to connect directly to a standard 36-way connector as shown:



The pinout numbering conventions are different for the two styles of connector (see diagram). However, the pinout is arranged to give a one to one connection to a 36-way delta printer connector when using Insulation Displacement Connectors (IDC) and ribbon cable.

Not all the signals defined for a 36 way connector are supported by the BVME4000/6000. The cable assembly should be built such that pin 1 on the 26 way connector connects to pin 1 of the 36 way. A 26 way ribbon cable is used leaving pins 14 - 18 and 32 - 36 unconnected.

Figure 18 JP3 Parallel Port Connections

6.3 JP4 Cheapernet Connector

JP4 provides a 50Ω BNC connection to a 'Cheapernet' (IEEE802.3 10Base2) network.

When connecting to a network it is important that the bus topology is preserved. The Cheapernet bus is a multidrop bus with 50Ω terminators at each end. Ideally each station on the bus has a zero length stub connecting from the cable to the transceiver in the station. In practice, connection to the cable is made using a BNC T-piece connected to the BNC connector. The cable is broken at the point of contact and each new end is connected to the T-piece.

If the BVME4000/6000 is to be removed from the network, this is simply accomplished by disconnecting the BVME4000/6000 BNC connector (JP4) from the T-piece, leaving the T-piece connected to the cable.

All cheapernet cabling should use RG-58 type cable. It is important to ensure that both ends of the cable are terminated using 50Ω BNC terminators.

Note: JP4 may be replaced by an optional 10BaseT RJ45 connection.

6.4 JP4 Optional 10BaseT Connector

The BVME4000/6000 may be fitted with an optional 10BaseT (twisted pair) Ethernet module. In this case the 10BaseT connection is permanently selected and the AUI is not available. The JP4 BNC connection is replaced with an RJ45 connector with the standard IEEE802.3 10BaseT pinout as shown:

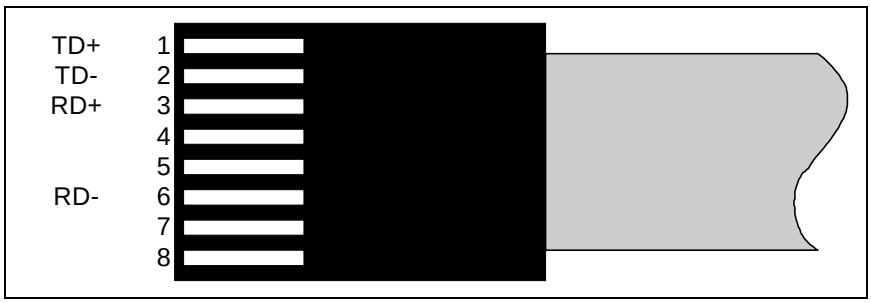


Figure 19 JP4 Optional 10BaseT Connector

6.5 JP5A/B IP A/B Connections

Each of the 50 pins on each I/O connector for the two IP, slots A and B, connects to a like-numbered pin on the two corresponding flat cable connectors, JP5A and JP5B on the BVME4000/6000 front panel. The IP I/O connector, the BVME4000/6000 flat cable connectors, and the wires on the ribbon cables are all numbered identically from 1 to 50.

Pin 1 on IP and BVME4000/6000 connectors are marked with a square pad, observable from the solder side of the respective board. Pin 1 is shown on JP5 by a triangle etched into the connector body. Pin 1 is typically marked on ribbon cable with a red stripe and on ribbon cable connectors with a manufacturer's mark, often a moulded textured triangle.

Caution: This consistent pin numbering system is not maintained with many mass-terminated connectors. Each type of connector has its own intrinsic pin numbering system. Systems integrators or users making their own cables must be certain which pin corresponds to which signal.

The pin assignment of the IP I/O connector is fixed by the connector manufacturer and repeated in the IP Specification. This assignment is shown below.

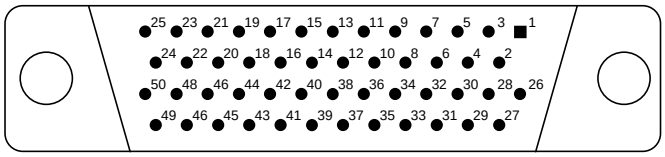


Figure 20 IP Connector Pin Numbering
Viewed from solder side of BVME4000/6000

The pin assignment of the 50-way flat cable connectors JA and JB are shown below:

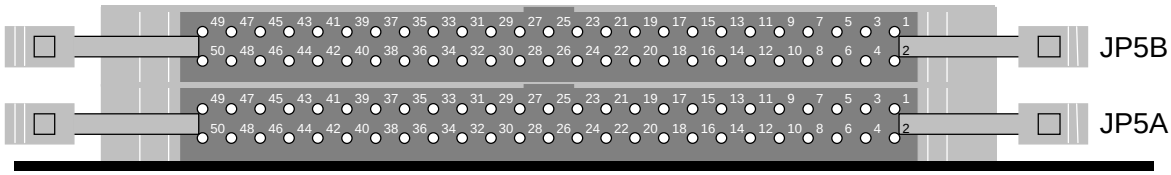
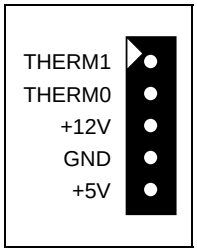


Figure 21 Flat Cable Connector Pin Numbering
Viewed from front of JP5

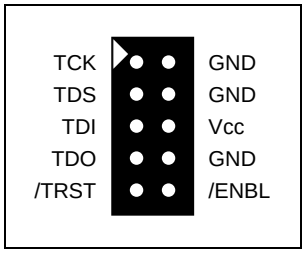
6.6 JP7 CPU Fan Power



JP7 is a power connection for a CPU fan (if fitted). Normally this will not be required, but in environments where the air-flow is not sufficient, the airflow can be supplemented in this way. When a 68060 series CPU is being used, it's thermal output signals for variable-speed fans are also available on this connector. Refer to "Appendix E Thermal Management (on page 68)" for more details.

Figure 22 JP7 CPU Fan Power

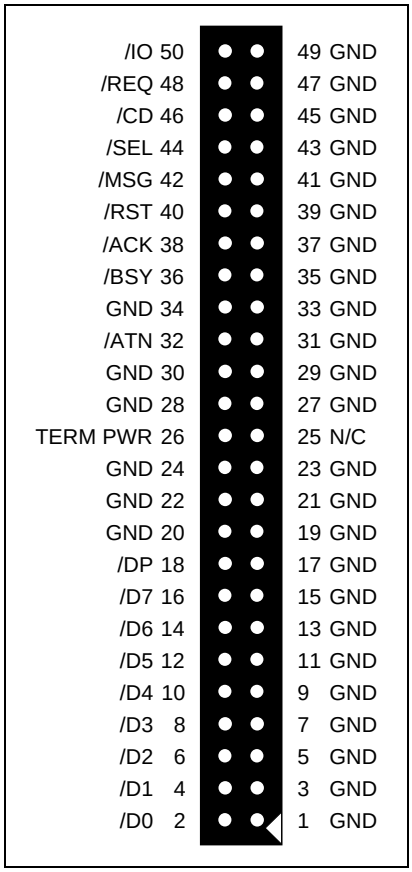
6.7 JP8 JTAG Connector



JP8 is a JTAG connection via a 2 x 5 way header, the pinout matching the MACH programming lead. This is for **factory use only**, to program the internal BVME4000/6000 logic devices.

Figure 23 JP8 JTAG Connector

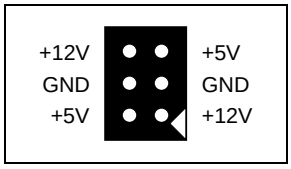
6.8 J1 SCSI Connections



J1 carries the SCSI interface signals. The connector pinout allows a 50 way IDC and ribbon cable assembly to be directly connected. If necessary a standard 50-pin to 68-pin SCSI-1 to SCSI-3 adapter may be used to adapt to 68-pin SCSI devices.

Figure 24 J1 SCSI Connections

6.9 J14 SCSI Peripheral Power Connections



J14 provides a power pick up connection for SCSI devices integrated within a module with the BVME4000/6000. It can provide up to 2A of +5V and 2A of +12V. The pinout is arranged to be symmetrical allowing the mating connector to be plugged either way around.

Figure 25 J14 SCSI Peripheral Power Connections

6.10 P2 I/O Connections

P2 is a 96 way, DIN-41612 connector consisting of 3 rows of 32 pins. The centre row (Row b) carries VMEbus 32-bit extension signals. The other two rows carry BVME4000/6000 specific I/O connections:

P2 Connection	Row a	Row c
1	TxDA	RxDA
2	RTSA	CTSA
3	DTRA	DCDA
4	SCLKOUTA	SCLKINA
5	TxDB	RxDB
6	RTSB	CTSB
7	DTRB	DCDB
8	SCLKOUTB	SCLKINB
9	+12V	GND
10	AUI-DO+	AUI-DO-
11	AUI-DI+	AUI-DI-
12	AUI-COLL+	AUI-COLL-
13	GND	GND
14	SCSI-IO	SCSI-REQ
15	SCSI-CD	SCSI-SEL
16	SCSI-MSG	SCSI-RES
17	SCSI-ACK	SCSI-BSY
18	SCSI-ATN	SCSI-TERM
19	GND	GND
20	SCSI-DP	SCSI-D7
21	SCSI-D6	SCSI-D5
22	SCSI-D4	SCSI-D3
23	SCSI-D2	SCSI-D1
24	SCSI-D0	GND
25	GND	+5V
26	PIO-7	PIO-6
27	PIO-5	PIO-4
28	PIO-3	PIO-2
29	PIO-1	PIO-0
30	/PIO-STRB	PIO-ACK
31	PIO-BUSY	GND
32	N/C	N/C

6.11 Protection Fuses

The connections on the BVME4000/6000 which provide output power are protected with fuses. These are surface-mounted fuses, and the BVME4000/6000 should be returned to factory for repair if any of these fuses blows. For reference, the following is a list of the fuses, their functions, positions, rating and type.

Location (see below)	Function	Rating	Type (LittleFuse)
F1	SCSI TERM PWR	1.5A	ALF II 42901.5
F2	ETHERNET -9V	200mA	ALF II 429.200
F3	J14 +5V	2A	ALF II 429002
F4	J14 +12V	2A	ALF II 429002
F5	IP A +12V	1A	ALF II 429001
F6	IP B +12V	1A	ALF II 429001
F7	IP B +5V	2A	ALF II 429002
F8	IP A -12V	1A	ALF II 429001
F9	IP B -12V	1A	ALF II 429001
F10	IP A +5V	2A	ALF II 429002

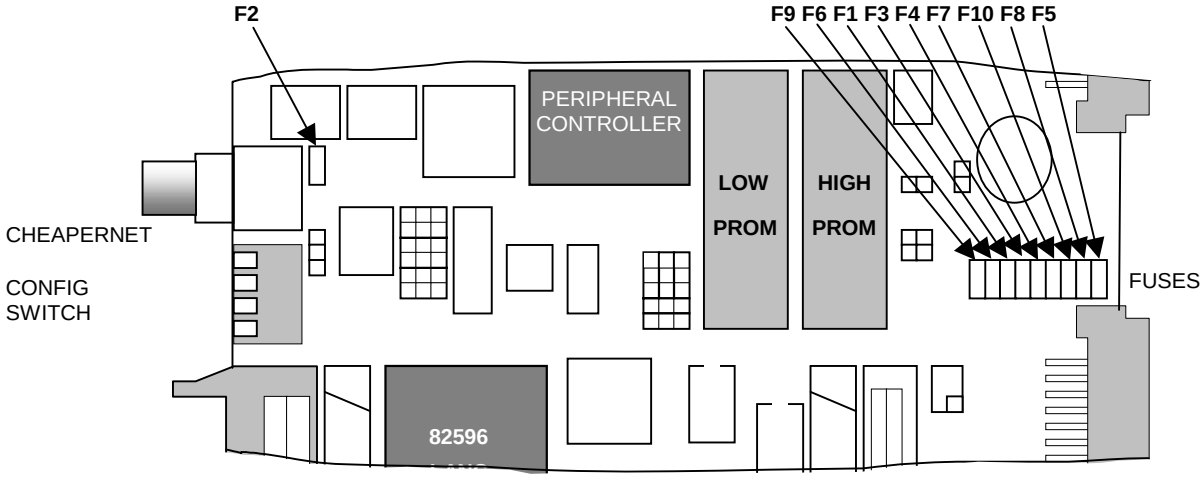


Figure 26 Protection Fuse Positions

7. Programming

7.1 Address Map

The Address Map for the BVME4000/6000 is shown below. The BVME4000/6000 is byte addressed; each location addresses an 8-bit value. The BVME4000/6000 supports full 32-bit addressing for all four Local Bus Masters (the MC68040/68060 CPU, the 82596CA LANC, the 53C710 SCSI Controller and the VMEbus Slave Interface).

Some devices (IP memory, EPROM, SRAM, VMEbus A24) are dual mapped. This is to allow the Transparent Translation registers in the MC68040/68060 to provide alternative cache modes for accesses to these devices. The Cache Mode column is suggested cache mode, the hardware provides no implicit cache mode control.

Address Range	Device	Size	Width	Cache Mode	Notes
00000000 - variable	Memory Module or SRAM	variable	D32	copyback	1,2,4,6
variable - CFFFFFFF	VMEbus - A32:D32	up to 3328Mb	D32	write through	2
D0000000 - DFFFFFFF	VMEbus - A32:D16	256Mb	D16	write through	
E0000000 - E7FFFFFF	IP Memory (up to 8 IPs)	128Mb	D16:D32	write through	5
E8000000 - E8FFFFFF	EPROM	16Mb (2Mb valid)	D16	write through	4,5
E9000000 - E9FFFFFF	SRAM (alternate)	16Mb (2Mb valid)	D32	write through	3,5
EA000000 - ECFFFFFF	Reserved	48Mb			
ED000000 - EDFFFFFF	VMEbus - A24:D32	16Mb	D32	write through	5
EE000000 - EEFFFFFF	VMEbus - A24:D16	16Mb	D16	write through	5
EF000000 - EFFFFFFF	Reserved	16Mb			
F0000000 - F7FFFFFF	IP Memory (up to 8 IPs)	128Mb	D16:D32	non-cached serial	5
F8000000 - F8FFFFFF	EPROM	16Mb (2Mb valid)	D16	non-cached serial	4,5
F9000000 - F9FFFFFF	SRAM (alternate)	16Mb (2Mb valid)	D32	non-cached serial	3,5
FA000000 - FCFFFFFF	Reserved	48Mb			
FD000000 - FDFFFFFF	VMEbus - A24:D32	16Mb	D32	non-cached serial	5
FE000000 - FEFFFFFF	VMEbus - A24:D16	16Mb	D16	non-cached serial	5
FF000000 - FFFFFFFF	I/O see I/O map	16Mb		non-cached serial	

NOTES:

1 If 'RAMLO' is set, then accesses to the bottom 512Kb/2Mb of this space access the Battery Backed SRAM.

2 The boundary between these spaces depends on how much memory is fitted to the memory module. Any space down here that is not decoded by the SRAM (if 'RAMLO' is set) or the memory module is decoded as a VMEbus A32:D32 access. This can be overridden if 'VMELO' is clear, in which case the bottom 256Mb are decoded as on-board (SRAM or memory module) accesses only.

3 If no memory module is fitted, this SRAM can be dual mapped, see note 1. The SRAM is always accessible at this location.

4 For the first two accesses after RESET the EPROM is dual mapped at 00000000.

5 These spaces are dual mapped in order to allow different caching modes to be set up using the MC68040/68060's Transparent Translation Registers.

6 The caching mode is programmable on 16Mb boundaries. Therefore if the amount of on board memory is not divisible by 16Mb, the bottom bit of the VMEbus A32:D32 space will have to be copy back cached. THIS MAY GIVE CACHE COHERENCY PROBLEMS as the processor is unable to snoop VMEbus space. In this case locate the VMEbus A32:D32 devices on a 16Mbyte boundary which will allow the transparent translation registers to be set up to give a coherent caching mode.

7.1.1 I/O Address Map

Address Range	Device	Size	Width
FF000000 - FF0FFFFF	SCSI Controller	1Mb	D32
FF100000 - FF1FFFFF	Ethernet Controller (LANC)	1Mb	D32
FF200000 - FF2FFFFF	Interrupt Control	1Mb	D8(OLW)
FF300000 - FF3FFFFF	IP Control	1Mb	D8(OLW)
FF400000 - FF4FFFFF	VME Slave Access Control	1Mb	D8(OLW)
FF500000 - FF5FFFFF	Configuration Switch	1Mb	D8(OLW)
FF600000 - FF7FFFFF	Reserved	2Mb	
FF800000 - FF8FFFFF	IP I/O/ID space (up to 8 IP's)	1Mb	D16:D32
FF900000 - FF9FFFFF	RTC	1Mb	D8(OLW)
FFA00000 - FFAFFFFF	Parallel Port	1Mb	D8(OLW)
FFB00000 - FFBFFFFF	SCC	1Mb	D8(OLW)
FFC00000 - FFDFFFFF	Reserved	2Mb	
FFE00000 - FFEFFFFF	VMEbus A16	1Mb (64K wraps)	D32
FFF00000 - FFFFFFFF	VMEbus A16	1Mb (64K wraps)	D16

7.2 Memory Module

Base Address : 00000000
Size : Memory Module Dependent.

The BVME4000/6000 provides a site for BVM Memory Modules - refer to "Appendix C Memory Module Pinout (on page 66)" for details. These modules are available in various configurations (DRAM, SRAM, FLASH) and sizes and access speeds. Refer to the relevant Memory Module documentation detailed in the "Appendix A Data Sheet & Manual References (on page 60)" section of this manual for details of the configuration.

The Memory Module Interface is 32-bits wide (though byte addressed) and supports Cache LINE transfers. Thus 'zero wait state' operation is supported; giving the MC68040/68060 optimum performance of 2/1/1/1 clock cycles per transfer. Thus 16 bytes of data can be transferred in 5 clock cycles (80Mbyte/sec @ 25MHz bus clock). Refer to the relevant Memory Module Manual for actual memory performance.

The Memory Module provides a 'memory present' (/MEMOK) signal during the first cycle of an access that it decodes. Thus the BVME4000/6000 address decoder automatically handles different size Memory Modules. Any accesses (for addresses up to CFFFFFFF) that are not decoded by the Memory Module, generate a VMEbus A32:D32 master access (except if VMELO is clear, in which case the bottom 256Mb are decoded as on-board accesses only) - refer to "7.3.6 A32:D32 (on page 28)" for more details.

7.3 VMEbus Master Access

The BVME4000/6000 can access VMEbus as a bus master. Depending on the Address Range used, different types of access are performed.

VMEbus specifies three basic Address Mode schemes - A16 (Short I/O), A24 (Standard) and A32 (Extended). The BVME4000/6000 supports all of these modes.

VMEbus also specifies three basic Data Transfer schemes - D08(EO), D16 and D32. The BVME4000/6000 supports all these modes.

The BVME4000/6000 does not support Block transfers or A64:D64.

7.3.1 A16:D16 (D08EO)

Base Address : FFFF0000.
Size : 64Kbyte.

Accesses to this area perform a Short I/O access to VMEbus with LWORD inactive. Line and Long Word accesses are automatically broken down to Word (D16) cycles. Byte accesses produce a D08(EO) cycle. These accesses only involve signals available on the P1 VMEbus Connector.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Data Access	=	$2D
CPU User	Data Access	=	$29

7.3.2 A16:D32

Base Address : FFEF0000.
Size : 64Kbyte.

Accesses to this area perform a Short I/O access to VMEbus with LWORD dependent on the access type. Line and Long Word accesses produce a D32 (LWORD active) cycle. Word accesses produce a D16 (LWORD inactive) cycle. Byte accesses produce a D08(EO) cycle. These accesses involve signals on both P1 and P2, therefore, a 'P2' Backplane is required.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Data Access	=	$2D
CPU User	Data Access	=	$29

7.3.3 A24:D16 (D08EO)

Base Address : FE000000 or EE000000.
Size : 16Mbyte.

Accesses to this area perform a Standard Address access to VMEbus with LWORD inactive. Line and Long Word accesses are automatically broken down to Word (D16) cycles. Byte accesses produce a D08(EO) cycle. These accesses only involve signals available on the P1 VMEbus Connector.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Program Access	=	$3E
	Data Access	=	$3D
CPU User	Program Access	=	$3A
	Data Access	=	$39

7.3.4 A24:D32

Base Address : FD000000 or ED000000.
Size : 16Mbyte.

Accesses to this area perform a Standard Address access to VMEbus with LWORD dependent on the access type. Line and Long Word accesses produce a D32 (LWORD active) cycle. Word accesses produce a D16 (LWORD inactive) cycle. Byte accesses produce a D08(EO) cycle. These accesses involve signals on both P1 and P2, therefore, a 'P2' Backplane is required.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Program Access	=	$3E
	Data Access	=	$3D
CPU User	Program Access	=	$3A
	Data Access	=	$39

7.3.5 A32:D16

Base Address : D0000000.
Size : 16Mbyte.

Accesses to this area perform an Extended Address access to VMEbus with LWORD inactive. Line and Long Word accesses are automatically broken down to Word (D16) cycles. Byte accesses produce a D08(EO) cycle. These accesses involve signals on both P1 and P2, therefore, a 'P2' Backplane is required.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Program Access	=	$0E
	Data Access	=	$0D
CPU User	Program Access	=	$0A
	Data Access	=	$09

7.3.6 A32:D32

Base Address : Immediately above the Memory Module, or 10000000 (if VMELO is clear).
Size : Maximum 3328Mbyte (Memory Module Dependent).

Accesses to this area perform a Standard Address access to VMEbus with LWORD dependent on the access type. Line and Long Word accesses produce a D32 (LWORD active) cycle. Word accesses produce a D16 (LWORD inactive) cycle. Byte accesses produce a D08(EO) cycle. These accesses involve signals on both P1 and P2, therefore, a 'P2' Backplane is required.

This address space can follow on contiguously from the top of a memory module, or the SRAM (if RAMLO is set), or can be set to start at a fixed base address (if VMELO is clear). This allows for a fixed partitioning of on-board and off-board memory for operating systems with this requirement. Refer to "7.10 VMEbus Slave Access Controller (on page 45)" for RAMLO and VMELO settings.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Program Access	=	$0E
	Data Access	=	$0D
CPU User	Program Access	=	$0A
	Data Access	=	$09

7.4 SRAM

Base Address : E9000000 or F9000000.
Size : 512K/2Mbyte.

The 512Kbytes or 2Mbytes of SRAM is 32-bits wide, and provides a 5 CPU clock cycle access. The SRAM can be accessed at the above two locations, which provide for different cache regions for the same memory. Normally the MC68040/68060 will be set-up so that accesses in the region E9000000 - E9FFFFFF are write-through cached, and accesses in the region F9000000 - F9FFFFFF are non-cached with bus-serialised access.

The SRAM is normally backed up by an on-board memory storage capacitor, and typically is used for non-volatile storage applications such as a RAM-disc. In this case, the SRAM can retain it's data for up to 7 days. If link selected to enable backup from the on-board battery, then the data can be retained for up to 2.5 years, allowing also for the supply to the Real Time Clock - see "5.2.11 LK21 SRAM Backup Selection (on page 17)". The SRAM is also backed-up from the VMEbus STDBY line. When using the VMEbus STDBY line, retention time is dependant on the external source.

The SRAM can also be mapped to appear at the bottom 512K/2Mbytes of the memory map for boards without a memory module fitted by setting RAMLO. In this case the SRAM is used as main system memory, and normally will be treated as copy-back cached memory for maximum performance. Refer to "7.10 VMEbus Slave Access Controller (on page 45)" for RAMLO setting.

7.5 EPROM

Base Address : E8000000 or F8000000.
Size : 2Mbyte.

The BVME4000/6000 provides 2 x 32-Pin EPROM JEDEC compatible sockets that may be link selected to accept either 64K8, 128K8, 512K8 or 1024K8 EPROM devices (e.g. 27C512, 27C010, 27C020, 27C040 or 27C080), providing 64K-2Mbytes of EPROM or 512K8 AM29F040 single-voltage FLASH EPROM devices, providing 1Mbyte of on-board programmable FLASH EPROM memory.

The EPROM space is 16-bits wide, and provides a 10 CPU clock cycle access. 90nS or faster devices must be used at 33MHz, 120nS devices may be used at 25MHz bus clock. The EPROM can be accessed at the above two locations, which provide for different cache regions for the same memory. Normally the MC68040/68060 will be set-up so that accesses in the region E8000000 - E8FFFFFF are write-through cached, and accesses in the region F8000000 - F8FFFFFF are non-cached with bus-serialised access.

The EPROM is also mapped at the bottom of the memory map for the first two cycles after a reset. This is to allow for the MC68040/68060 to fetch the initial program counter and stack pointer from the first two longword locations in the EPROM.

When AM29F040 devices are fitted in these sockets, they can be accessed word-wide for programming, erasing etc.. This means that effectively the sector sizes are 128Kbytes (64Kbytes per device), and they can be programmed/erased in parallel. For full programming details, refer to the AMD AM29F040 documentation detailed in the "A.10 AM29F040 (on page 60)" section of this manual.

7.6 SCSI Controller

7.6.1 Overview

The SCSI Interface uses the NCR53C710. This provides asynchronous transfers of up to 5Mbytes per second and synchronous transfers of up to 10Mbytes per second. The 32-bit DMA driven interface allows direct access to the entire memory map of the BVME4000/6000. The burst mode interface stacks up 16 bytes at a time and transfers them as a line transfer at up to 4/2/2/2 access speeds at 25MHz bus clock. This gives a 400nS burst every 3.2µS (at 5Mbyte/s) or 12.5% bus bandwidth requirement.

The 53C710 is an intelligent Processor in its own right, running SCSI SCRIPTS software. This enables very high level commands to be issued to the SCSI interface further minimising processor overhead.

7.6.2 Programming

The 53C710 is controlled using the 64 registers defined in section "7.6.4 SCSI Controller Registers (on page 31)". Transfers with the SCSI bus are conducted independently of the main CPU. The main CPU sets up various parameters in the 53C710's registers, points the 53C710 at the start of a SCSI SCRIPTS routine and tells it to run. Upon termination the 53C710 interrupts the main CPU and waits for a new start address. The main CPU can examine the results of the operation by interrogating the 53C710 registers.

The 53C710 can access the entire BVME4000/6000 address space, including becoming VMEbus master. It accesses memory for two purposes: SCRIPTS code fetches and DMA accesses for SCSI data transfers.

Note that the 53C710 is configured for Big Endian Mode. This can affect addressing in fairly subtle ways. For full programming details, refer to the 53C710 documentation detailed in the "A.4 53C710 (on page 60)" section of this manual.

Refer to "Appendix B CPU Cache Coherency and Bus Snooping (on page 62)" for details on Cache Coherency Implications (snooping) while the 53C710 is a bus master.

Refer to "7.8 Interrupt Controller (on page 35)" for details of Interrupt generation by the 53C710.

7.6.3 Hardware Specific Considerations

The raw SCSI clock (SCLK) is driven with 40MHz. Thus the CF(1-0) bits in the DCNTL register must be set to 00 (default value). This gives a core clock of 20MHz and a SCSI-1 synchronous transfer rate of 5Mb/s. Optionally, the SSCF(1-0) bits in the SBCL may be set to 01 to give a SCSI-2 synchronous transfer rate of 10Mb/s.

The 53C710 is hardware configured for Bus Mode 2. The following need to be set for correct operation of the bus interface:

The first access to the 53C710 must be to set EA bit in DCNTL (This enables the 53C710 to generate TA for slave cycles).
The TT1 bit of CTEST7 must be set (indicates TT1 pin cleared when bus master).
The TT0 bit of DMODE must be clear (indicates TT0 pin cleared when bus master).
The FC(2-1) bits of DMODE should be set to 10 (indicates Supervisor Data Access).
The PD bit of DMODE should always be clear (indicating Supervisor Data for all accesses).
The SM bit of CTEST8 must be clear (snoop control only driven as master).
The FA bit of DCNTL should always be clear (no 'fast' arbitration).

The BVME4000/6000 does not support differential SCSI transfers thus the DIFF bit of CTEST7 must always be clear.

7.6.4 SCSI Controller Registers

Address	Size	Read Write	Register	Description
FF000000	B	R/W	SIEN	SCSI Interrupt Enable
FF000001	B	R/W	SDID	SCSI Destination ID
FF000002	B	R/W	SCNTL1	SCSI Control 1
FF000003	B	R/W	SCNTL0	SCSI Control 0
FF000004	B	R/W	SOCL	SCSI Output Control Latch
FF000005	B	R/W	SODL	SCSI Output Data Latch
FF000006	B	R/W	SXFER	SCSI Transfer
FF000007	B	R/W	SCID	SCSI Chip ID
FF000008	B	R/W	SBCL	SCSI Bus Control Lines
FF000009	B	R	SBDL	SCSI Bus Data Lines
FF00000A	B	R	SIDL	SCSI Input Data Latch
FF00000B	B	R/W*	SFBR	SCSI First Byte Received (Write Restrictions apply)
FF00000C	B	R	SSTAT2	SCSI Status 2
FF00000D	B	R	SSTAT0	SCSI Status 1
FF00000E	B	R	SSTAT0	SCSI Status 0
FF00000F	B	R	DSTAT	DMA Status
FF000010	LW	R/W	DSA	Data Structure Address
FF000014	B	R	CTEST3	Chip Test 3
FF000015	B	R	CTEST2	Chip Test 2
FF000016	B	R	CTEST1	Chip Test 1
FF000017	B	R/W	CTEST0	Chip Test 0
FF000018	B	R/W	CTEST7	Chip Test 7
FF000019	B	R/W	CTEST6	Chip Test 6
FF00001A	B	R/W	CTEST5	Chip Test 5
FF00001B	B	R/W	CTEST4	Chip Test 4
FF00001C	LW	R/W	TEMP	Temporary Stack
FF000020	B	R/W	LCRC	Longitudinal Parity
FF000021	B	R/W	CTEST8	Chip Test 8
FF000022	B	R/W	ISTAT	Interrupt Status
FF000023	B	R/W	DFIFO	DMA FIFO
FF000024	B	R/W	DCMD	DMA Command
FF000025	(B)	R/W	DBC (lsb)	DMA Byte Counter (least significant byte)
FF000026	W	R/W	DBC	DMA Byte Counter
FF000028	LW	R/W	DNAD	DMA Next Address for Data
FF00002C	LW	R/W	DSP	DMA SCRIPTS Pointer
FF000030	LW	R/W	DSPS	DMA SCRIPTS Pointer Save
FF000034	LW	R/W	SCRATCH	General Purpose Scratch Pad
FF000038	B	R/W	DCNTL	DMA Control
FF000039	B	R/W	DWT	DMA Watchdog Timer
FF00003A	B	R/W	DIEN	DMA Interrupt Enable
FF00003B	B	R/W	DMODE	DMA Mode
FF00003C	LW	R/W	ADDER	Sum Output of Internal Adder

7.6.5 SCSI Electrical Interface

The output drivers for the SCSI interface fully conform to the electrical requirements of SCSI-1 and SCSI-2.

The drivers are isolated from the power supply. This ensures that, when powered down, the BVME4000/6000 does not affect the active SCSI bus.

The SCSI bus requires termination at both ends of the bus. It is important that terminators are fitted at, and only at, both ends of the bus. The BVME4000/6000 uses active, current-mode terminators that provide high performance termination that allows the BVME4000/6000 to achieve 10Mb/s transfer rates when connected to a SCSI-2 bus.

The BVME4000/6000 terminators are active when LK13 is omitted. When LK13 is fitted, then the BVME4000/6000 terminators are completely disabled and provide no load to the SCSI bus.

The BVME4000/6000 drives TERMPWR and uses TERMPWR for its onboard terminators. Thus even when unpowered the BVME4000/6000 will provide correct termination, if enabled (LK13 omitted).

Connection to SCSI bus is achieved via two alternative connections:

1. J1 provides a direct connection to a 50-way standard IDC ribbon. The layout of this connector is intended for direct connection to SCSI peripherals built into a module with the BVME4000/6000.

2. P2 carries all the SCSI signals (including TERMPWR). This allows a transition module to be connected behind the backplane to provide connection to SCSI peripherals outside the BVME4000/6000 enclosure.

Refer to section "6 Connector Pinouts (on page 19)" for details of SCSI connector pinouts.

7.7 Ethernet Controller

7.7.1 Overview

The Ethernet Interface is built around the Intel 82596CA LANC. This provides a 32-bit DMA driven interface to both Ethernet (via the AUI interface) and Cheapernet (via a front panel BNC). The 32-bit, DMA driven interface allows direct access to the entire memory map of the BVME4000/6000 allowing full packet management by the 82596CA. Each 32-bit transfer requires 320nS max (including arbitration) to execute the cycle. A transfer will occur no more frequently than every 4µS (4 bytes at 1Mbyte per second). Thus worst case bus bandwidth requirement is 8% at 25MHz bus clock.

7.7.2 Programming

The CPU and the 82596CA do not communicate directly (by registers). Instead, they communicate via a shared memory model. That is, the CPU sets up command blocks in memory and activates the 82596CA's Channel Attention. The 82596CA then examines the command block and executes the commands. When it has finished it generates an interrupt to the CPU.

The 82596CA is hardware configured for Big Endian operation. This has fairly subtle effects on parameter ordering in memory command blocks; in particular, most address pointers have their words swapped. For full programming details, refer to the 82596CA documentation detailed in the "A.3 82596CA (on page 60)" section of this manual.

Although the CPU and the 82596CA do not generally communicate directly, there is a 'virtual' register that the CPU can access to assert Channel Attention and to write to an 82596CA internal register (PORT).

Refer to "Appendix B CPU Cache Coherency and Bus Snooping (on page 62)" for details on Cache Coherency Implications (snooping) while the 82596CA is a bus master.

Refer to "7.8 Interrupt Controller (on page 35)" for details of Interrupt generation by the 82596CA.

7.7.3 PORT Access

Accesses to the PORT register consist of **two consecutive 32-bit writes** at location **FF100000**, with bits D31..D16 of the command in the least significant word and bits D15..D0 of the command in the most significant word (i.e. the command is word-swapped). The PORT register is a write only register.

Writing to the 82596CA PORT allows the CPU to do four things:

1. Write an Alternative System Configuration Pointer (SCP) address. This needs to be done as the 82596CA will, by default, access 00FFFFF6 for its initial command block after reset.

2. Perform a dump of the internal state of the 82596CA to a specified address.

3. Execute a software reset.

4. Execute a self-test and write the results to memory at the specified address.

Function	D31	D4	D3	D2	D1	D0
Reset			0	0	0	0
Self-Test	A31 Self-test Results Area	A4	0	0	0	1
SCP	A31 Alternative SCP Address	A4	0	0	1	0
Dump	A31 Dump Area Pointer	A4	0	0	1	1

7.7.4 Channel Attention Access

Reading from location **FF100000** causes a pulse on the 82596CA Channel Attention input. This causes the 82596CA to execute command blocks.

7.7.5 Bus Error Handling

The 82596CA cannot directly handle bus errors. If the 82596CA is the bus master and accesses a location from which a bus error is generated (e.g. accesses non-existent memory) then special hardware on the BVME4000/6000 handles the error condition.

When a bus error occurs, the 82596CA is removed from the bus and kept off the bus by asserting BOFF. ETHERR is generated causing an Ethernet Interrupt and the ETHERR bit to be set in the Interrupt Local Status Register - refer to "7.8 Interrupt Controller (on page 35)" for details of interrupt control and status. The 82596CA is held off the bus until a reset PORT command is issued to the 82596CA.

7.7.6 SYSBUS Byte Requirements

The SYSBUS byte of the SCP controls various hardware bus operations and must be set up as follows:

	Bit 6	Must be set.
INT	Bit 5	Must be clear (active high interrupt).
LOCK	Bit 4	LOCKed cycles are supported on the BVME4000/6000. It is recommended that the LOCK function be enabled (bit is clear).
TRG	Bit 3	External Triggering is supported on the BVME4000/6000. It is recommended that external triggering be used (bit is set).
M(1-0)	Bit 2,1	Should only be used in Linear Addressing Mode (bit 2 is set, bit 1 is clear).

7.7.7 Electrical Interface

The BVME4000/6000 provides both a full 'Cheapernet' (IEEE802.3 - 10Base2) coaxial interface via the front panel and an Attachment Unit Interface (AUI) port via P2. This allows a transition module to be connected behind the backplane to provide connection to Thick Ethernet (IEE802.3 - 10Base5) or other Ethernet standards (e.g. Twisted Pair IEE802.3 - 10BaseT) outside the BVME4000/6000 enclosure.

Selection between the on board Cheapernet interface or the P2 AUI connection is made by three links - refer to "5.2.7 LK7,8,9 Ethernet AUI/Cheapernet Select (on page 15)" for details of the link settings.

An optional 10BaseT (twisted pair) module is available which replaces the Cheapernet connection. The AUI port is not available when this module is fitted.

7.8 Interrupt Controller

7.8.1 Overview

The Interrupt Controller is responsible for two independent functions:

Processor Interrupter - Takes interrupts from all sources (including VMEbus IRQ's, IP IRQ's, Timers, etc.) and generates an interrupt to the CPU.

VMEbus Interrupter - Generates Interrupts on the VMEbus.

7.8.2 Processor Interrupter

Interrupt Source	Level	Type
ABORT Switch	7	Auto-vectored
8570 Timers	6	Auto-vectored
68230 Timer	5	Vectored
Memory Module	4	Auto-vectored
85230 DUART	3	Vectored
53C710 SCSI	3	Auto-vectored
68230 Parallel	2	Vectored
82596CA ENET	2	Auto-vectored
Location Monitor	1	Auto-vectored
IP A Int 0	Program	Vectored - Level Programmable in IP Interface - see "7.9.6 IP Controller Registers (on page 42)".
IP A Int 1		
IP B Int 0		
IP B Int 1		
IP Daughter Board Interrupts, up to 12 sources	Program	Vectored - Level Programmable on IP Daughter Board.
VMEbus IRQ 7	7	Vectored - Individually maskable - see "7.8.4.1 VMEIRQ Enable Register (on page 36)".
VMEbus IRQ 6	6	
VMEbus IRQ 5	5	
VMEbus IRQ 4	4	
VMEbus IRQ 3	3	
VMEbus IRQ 2	2	
VMEbus IRQ 1	1	
VMEbus ACFAIL	7	Auto-vectored

Where multiple sources are generating interrupts on the same level, the acknowledge cycle is prioritised as follows:

Highest Priority: Auto-vectored
Local vectored
VMEbus Interrupt
Lowest Priority: IP

The IP Interrupts are highly programmable. They are programmed in the IP Interface - refer to "7.9 IP Controller (on page 39)" for details. The IP interface is responsible for prioritising any pending IP interrupts. The Interrupt Controller combines the current state of IP interrupts with all other sources to generate an Interrupt code to the CPU. During acknowledge cycles, the Interrupt Controller prioritises between sources of active interrupts and generates the appropriate acknowledge signal. If it acknowledges the IP interrupt, then the IP Interface prioritises between any active IP interrupts.

When a VMEbus Interrupt is acknowledged, the BVME4000/6000 becomes a VMEbus master and initiates an Interrupt Acknowledge cycle over VMEbus. The BVME4000/6000 expects the VMEbus interrupter to return a vector which is then used by the processor vectoring mechanism. If no VMEbus interrupter responds within the VMEbus time-out period, then a 'spurious interrupt' vector is generated.

7.8.3 VMEbus interrupter

The BVME4000/6000 can generate interrupts on the VMEbus. This function is completely independent of the processor Interrupter function. When acknowledged by the VMEbus interrupt handler, the BVME4000/6000 returns a programmable 8-bit vector. The interrupter is implemented as Release On AcKnowledge (ROAK). Thus the interrupt is cleared by the interrupt acknowledge cycle.

The BVME4000/6000 may generate an interrupt on any of the seven VMEbus IRQ levels. However, it can only generate on a single level at any one time. The level on which an interrupt is generated is programmable - refer to "7.8.4.2 VMEIRQ Vector Register (below)" for details.

The interrupt is asserted by the processor writing to the VMEIRQ Vector Register - refer to "7.8.4.3 VMEIRQ Level Register (on page 37)" for details. The value written to the VMEIRQ Vector Register is then used as the value returned in the subsequent acknowledge cycle.

7.8.4 Interrupt Controller Registers

The Interrupt Controller contains six byte wide registers in four I/O locations. The first three locations are WRITE ONLY - DO NOT READ FROM THEM, the last location is READ ONLY.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF200003	VMEIRQ Enable	VIEN7	VIEN6	VIEN5	VIEN4	VIEN3	VIEN2	VIEN1	ACFEN
FF200007	VMEIRQ Vector	VEC7	VEC6	VEC5	VEC4	VEC3	VEC2	VEC1	0
	VMEIRQ Level	Rsrvd	Rsrvd	Rsrvd	Rsrvd	VLVL2	VLVL1	VLVL0	1
FF20000B	LOCIRQ Enable	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	LOCEN	0
	ETHIRQ Enable	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	ETHEN	1
FF20000F	Local IRQ Status	Rsrvd	Rsrvd	Rsrvd	Rsrvd	ABORT	ACFAIL	ETHERR	ETHIRQ

7.8.4.1 VMEIRQ Enable Register

Bit 7-1: **VIEN(7-1): VMEbus Interrupt Enable.**
When SET these bits enable the corresponding interrupts from VMEbus. For example setting bits 7 and 3 enable VMEbus IRQ's 7 and 3 to generate interrupts to the processor.

After RESET these bits are CLEAR (i.e. all VMEbus interrupts disabled).

Bit 0: **ACFEN: ACFAIL Interrupt Enable.**
When SET this bit enables interrupts from the VMEbus ACFAIL signal - refer to "7.8.4.6 Local IRQ Status Register (on page 38)" for details on ACFAIL interrupt operation.

After RESET this bit is CLEAR (i.e. ACFAIL interrupts disabled).

7.8.4.2 VMEIRQ Vector Register

Bit 7-1: **VEC(7-1): Interrupt Vector.**
Writing to this register sets bits 7 to 1 of the Interrupt ID vector that will be returned to the VMEbus Interrupt Handler, bit 0 is always set to ZERO. The act of writing to this register also causes the VMEbus interrupt line, selected by the LVL(2-0) bits in the VMEIRQ Level Register, to become active.

Bit 0: **Select Bit.**
This bit is used to select between the VMEIRQ Level Register and the VMEIRQ Vector Register. This bit must be written as a **ZERO** to select the VMEIRQ Vector Register.

7.8.4.3 VMEIRQ Level Register

Bit 7-4: **Reserved.**
For future compatibility these must be always written as zero.

Bit 3-1: **VLVL(2-0): VMEbus Interrupter Level.**
These bits select on which VMEbus Interrupt level the board will act as an interrupter. The binary code written selects the corresponding interrupt level (i.e. 101 selects level 5). When set to 000 no interrupt can be generated on VMEbus.

After RESET these bits are CLEAR (i.e. VMEbus interrupt generation disabled).

Bit 0: **Select Bit.**
This bit is used to select between the VMEIRQ Level Register and the VMEIRQ Vector Register. This bit must be written as **ONE** to select the VMEIRQ Level Register.

7.8.4.4 LOCIRQ Enable Register

Bit 7-2: **Reserved.**
For future compatibility these must be always written as zero.

Bit 1: **LOCEN: Location Monitor Interrupt Enable.**
When SET this bit enables interrupts from the VMEbus Location Monitor - refer to "7.10 VMEbus Slave Access Controller (on page 45)" for details of VMEbus Slave Operation.

After RESET this bit is CLEAR (i.e. location monitor interrupts disabled).

This bit is used to clear the Location Monitor Interrupt during interrupt service routines. The interrupt is cleared by disabling (CLEARing) and re-enabling (SETting) the Location Monitor Interrupt.

Bit 0: **Select Bit.**
This bit is used to select between the LOCIRQ Enable Register and the ETHIRQ Enable Register. This bit must be written as **ZERO** to select the LOCIRQ Enable Register.

7.8.4.5 ETHIRQ Enable Register

Bit 7-2: **Reserved.**
For future compatibility these must be always written as zero.

Bit 1: **ETHEN: Ethernet Interrupt Enable.**
When SET this bit enables interrupts from the 85296 Ethernet Controller - refer to "7.7 Ethernet Controller (on page 33)" for details of Ethernet Controller Operation.

After RESET this bit is CLEAR (i.e. 82596CA interrupts disabled).

This bit is used to clear the 82596CA Interrupt during interrupt service routines. The interrupt is cleared by disabling (CLEARing) and re-enabling (SETting) the Ethernet Interrupt.

Bit 0: **Select Bit.**
This bit is used to select between the LOCIRQ Enable Register and the ETHIRQ Enable Register. This bit must be written as a **ONE** to select the ETHIRQ Enable Register.

7.8.4.6 Local IRQ Status Register

Bit 7-4: **Reserved.**
These bits are unused. When read, their state is undefined.

Bit 3: **ABORT: Abort Switch Interrupt.**
This bit indicates the status of the ABORT switch. If this bit is SET the ABORT switch is pressed. This will also generate an Auto-vector level 7 interrupt, so this bit can be used to determine that the ABORT switch was the source of an Auto-vector level 7 interrupt.

Bit 2: **ACFAIL: VMEbus ACFAIL Interrupt.**
This bit indicates the status of the VMEbus ACFAIL signal. If this bit is SET the ACFAIL signal is active. This will also generate an Auto-vector level 7 interrupt, so this bit can be used to determine that the ACFAIL signal was the source of an Auto-vector level 7 interrupt.

Bit 1: **ETHERR: Ethernet ERROR Interrupt.**
This bit indicates that a 82596CA Ethernet Controller BUS ERROR has occurred - refer to "7.7.5 Bus Error Handling (on page 34)" for more details.

Bit 0: **ETHIRQ: Ethernet Interrupt Level.**
This bit indicates the status of the 82596CA Ethernet Controller interrupt signal. If this bit is SET the 82596CA's interrupt signal is active. **Note:** This does not indicate the status of the internal interrupt signal controlled by ETHEN, but indicates the status of the 82596CA's interrupt signal directly. The 82596CA will pulse its interrupt line inactive whenever a 'new' interrupt condition becomes true within the device. Thus to distinguish between an Ethernet Error interrupt and a normal Ethernet interrupt, the ETHERR bit should be interrogated; not the ETHIRQ bit.

7.9 IP Controller

7.9.1 Overview

The IP interface supports two onboard IP sites (IP A & IP B) as well as up to a further 4 IP sites via an expansion interface on a separate daughter board (IP's C to F).

Double width (D32) pairs of IP's are supported. Support for D16 and D32 Memory IP's is included.

High speed operation is supported:

8 MHz: This is the standard clock speed that all IP's support.

32 MHz: This higher speed operation is defined in the IP Specification. Many modern IP designs offer this higher speed operation.

SYNC: In this mode, the IP runs synchronously with the main CPU clock speed. This can achieve much higher performance on compatible IP's as clock synchronisation is not necessary.

7.9.2 IP Expansion Interface

The IP expansion interface allows for a low cost IP carrier daughter board to be added - refer to "Appendix D IP Expansion Interface Pinout (on page 67)" for details. The BVME4000/6000 contains all the state machine and multiplexing logic thus minimising daughter board circuitry requirements. The interface allows up to four additional IP sites on a daughter board at all speed selections. For example the EXP100 Expansion Board can be used - refer to the EXP100 documentation detailed in the to "A.16 EXP100 Quad IP Expansion User's Manual (on page 61)" section of this manual.

7.9.3 IP Interrupts

Each IP can generate interrupts on two separate IRQ lines, INT0 and INT1. The IP Interface contains registers for setting, in software, the level on which each IRQ source will generate interrupts. IRQ's from the on board IP's (i.e. first two) are supported in the IP interface. The daughter board is responsible for prioritising any pending interrupts from IP's on the daughter board. The IP interface combines the current state of the daughter board with that of onboard IP's to generate an interrupt code to the Interrupt Controller - refer to "7.8 Interrupt Controller (on page 35)" for details.

7.9.4 Memory Space Address Map

The Address Map logic decodes two 128Mbyte regions for memory space accesses, generating /IPMEMCS when the processor accesses either of the IP Memory regions. The IP memory is dual mapped in two regions to provide for accesses using different caching modes. Refer to "Appendix B CPU Cache Coherency and Bus Snooping (on page 62)" for more details. This region is then further decoded in the IP Interface.

Each IP can be accessed in two ways:

1. As a single, 16-bit wide device through an 8Mbyte window.

2. As a double-size, 32-bit wide device through a 16Mbyte window. In this mode, a pair of IP sites are used to take the double-size IP.

Thus A26 to A0 are used by the IP's or IP Interface for memory space decoding as shown below.

Address Range	A[26:23]	Size	IP Selected	IP A[22-A1]
E0000000 - E07FFFFF F0000000 - F07FFFFF	0000	8Mb (D16)	IP A	A22 - A1
E0800000 - E0FFFFFF F0800000 - F0FFFFFF	0001	8Mb (D16)	IP B	A22 - A1
E1000000 - E17FFFFF F1000000 - F17FFFFF	0010	8Mb (D16)	IP C	A22 - A1
E1800000 - E1FFFFFF F1800000 - F1FFFFFF	0011	8Mb (D16)	IP D	A22 - A1
E2000000 - E27FFFFF F2000000 - F27FFFFF	0100	8Mb (D16)	IP E	A22 - A1
E2800000 - E2FFFFFF F2800000 - F2FFFFFF	0101	8Mb (D16)	IP F	A22 - A1
E3000000 - E3FFFFFF F3000000 - F3FFFFFF	0110	16Mb (D16)	Reserved	don't care
E4000000 - E4FFFFFF F4000000 - F4FFFFFF	100x	16Mb (D32)	IP A/B	A23 - A2
E5000000 - E5FFFFFF F5000000 - F5FFFFFF	101x	16Mb (D32)	IP C/D	A23 - A2
E6000000 - E6FFFFFF F6000000 - F6FFFFFF	110x	16Mb (D32)	IP E/F	A23 - A2
E7000000 - E7FFFFFF F7000000 - F7FFFFFF	111x	16Mb (D32)	Reserved	don't care

7.9.5 I/O & ID Space Address Map

The address map logic decodes a 1Mbyte space of the I/O region to IP I/O. This space is shared amongst the 8 IP's.

Each IP has an I/O space consisting of 128 bytes mapped as 64 words. Also each IP has 128 bytes of ID space, this again is word mapped.

In addition each pair of IP's can be combined to give 32-bit wide accesses, as for memory accesses.

Address Range	A[11:7]	Size	IP Selected	IP A[6-1]
FF800000 - FF80007F	0000 0	128 byte (D16)	IP A I/O	A6 - A1
FF800080 - FF8000FF	0000 1	128 byte (D16)	IP A ID	A6 - A1
FF800100 - FF80017F	0001 0	128 byte (D16)	IP B I/O	A6 - A1
FF800180 - FF8001FF	0001 1	128 byte (D16)	IP B ID	A6 - A1
FF800200 - FF80027F	0010 0	128 byte (D16)	IP C I/O	A6 - A1
FF800280 - FF8002FF	0010 1	128 byte (D16)	IP C ID	A6 - A1
FF800300 - FF80037F	0011 0	128 byte (D16)	IP D I/O	A6 - A1
FF800380 - FF8003FF	0011 1	128 byte (D16)	IP D ID	A6 - A1
FF800400 - FF80047F	0100 0	128 byte (D16)	IP E I/O	A6 - A1
FF800480 - FF8004FF	0100 1	128 byte (D16)	IP E ID	A6 - A1
FF800500 - FF80057F	0101 0	128 byte (D16)	IP F I/O	A6 - A1
FF800580 - FF8005FF	0101 1	128 byte (D16)	IP F ID	A6 - A1
FF800600 - FF8007FF	011X X	512 byte (D16)	Reserved	don't care
FF800800 - FF8008FF	1000 X	256 byte (D32)	IP A/B I/O	A7 - A2
FF800900 - FF8009FF	1001 X	256 byte (D32)	IP C/D I/O	A7 - A2
FF800A00 - FF800AFF	1010 X	256 byte (D32)	IP E/F I/O	A7 - A2
FF800B00 - FF800BFF	1011 X	256 byte (D32)	Reserved	don't care
FF800C00 - FF800FFF	11XX X	1024 byte	Reserved	don't care
FF801000 - FF8FFFFF	XXXX X	1Mbyte minus 4Kbyte	Reserved *	

* NOTE: The address space FF801000 - FF8FFFFF is a wrap-around region of the FF800000 - FF800FFF address space.

7.9.6 IP Controller Registers

The IP Interface contains six byte wide registers. All registers are write only.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF300003	IRQ Level A0	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	A0L2	A0L1	A0L0
FF300083	IRQ Level A1	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	A1L2	A1L1	A1L0
FF300103	IRQ Level B0	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	B0L2	B0L1	B0L0
FF300183	IRQ Level B1	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	B1L2	B1L1	B1L0
FF300203	Clock Speed Select	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	CLKX	CLKB	CLKA
FF300283	SYNC Clock Select	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	SYNCX	SYNCB	SYNCA

7.9.6.1 IRQ Level A0 Register

Bit 7-3: **Reserved.**
For future compatibility these must be always written as zero.

Bit 2-0: **A0L(2-0): IP A IntReq 0 Level.**
These bits select on which Interrupt level the IP IntReq will act as an interrupter. The binary code written selects the corresponding interrupt level (e.g. 101 selects level 5). When set to 000 no interrupt can be generated.

After RESET these bits are CLEAR (i.e. interrupt generation disabled).

7.9.6.2 IRQ Level A1 Register

Bit 7-3: **Reserved.**
For future compatibility these must be always written as zero.

Bit 2-0: **A1L(2-0): IP A IntReq 1 Level.**
These bits select on which Interrupt level the IP IntReq will act as an interrupter. The binary code written selects the corresponding interrupt level (e.g. 100 selects level 4). When set to 000 no interrupt can be generated.

After RESET these bits are CLEAR (i.e. Interrupt generation disabled).

7.9.6.3 IRQ Level B0 Register

Bit 7-3: **Reserved.**
For future compatibility these must be always written as zero.

Bit 2-0: **B0L(2-0): IP B IntReq 0 Level.**
These bits select on which Interrupt level the IP IntReq will act as an interrupter. The binary code written selects the corresponding interrupt level (e.g. 011 selects level 3). When set to 000 no interrupt can be generated.

After RESET these bits are CLEAR (i.e. Interrupt generation disabled).

7.9.6.4 IRQ Level B1 Register

Bit 7-3: **Reserved.**
For future compatibility these must be always written as zero.

Bit 2-0: **B1L(2-0): IP B IntReq 1 Level.**
These bits select on which Interrupt level the IP IntReq will act as an interrupter. The binary code written selects the corresponding interrupt level (e.g. 010 selects level 2). When set to 000 no interrupt can be generated.

After RESET these bits are CLEAR (i.e. Interrupt generation disabled).

7.9.6.5 IP Clock Speed Select Register

The IP controller supports four different clock speeds to the IP sites: Two standard frequencies; 8MHz and 32MHz and two 'Source Synchronous' frequencies that are derived from the CPU clock. This register selects between the high speed (32MHz or CPU clock frequency) and low speed (8MHz or CPU clock divided by four). It is set up in conjunction with the IP Sync Clock Select Register to set the required IP frequency.

Bit 2: **CLKX: IP Expansion Interface Clock Select.**
When CLEAR the IP expansion interface is clocked at 8MHz or CPU Clock divided by four (depending on the setting of SYNCX bit of the IP SYNC Clock Select Register). When SET the IP expansion interface is clocked at 32MHz or CPU Clock (depending on the setting of SYNCX bit of the IP SYNC Clock Select Register).

After RESET this bit is CLEAR (i.e. 8MHz clock selected or CPU Clock divided by four).

Bit 1: **CLKB: IP B Clock Select.**
When CLEAR IP B is clocked at 8MHz or CPU Clock divided by four (depending on the setting of SYNCX bit of the IP SYNCB Clock Select Register). When SET the IP expansion interface is clocked at 32MHz or CPU Clock (depending on the setting of SYNCB bit of the IP SYNC Clock Select Register).

After RESET this bit is CLEAR (i.e. 8MHz clock selected or CPU Clock divided by four).

Bit 0: **CLKA: IP A Clock Select.**
When CLEAR IP A is clocked at 8MHz or CPU Clock divided by four (depending on the setting of SYNCX bit of the IP SYNCA Clock Select Register). When SET the IP expansion interface is clocked at 32MHz or CPU Clock (depending on the setting of SYNCA bit of the IP SYNC Clock Select Register).

After RESET this bit is CLEAR (i.e. 8MHz clock selected or CPU Clock divided by four).

7.9.6.6 IP SYNC Clock Select Register

The IP controller supports four different clock speeds to the IP sites. Two standard frequencies: 8MHz and 32MHz and two 'Source Synchronous' frequencies that are derived from the CPU clock. This register selects between the standard speed (32MHz or 8MHz) and Source Synchronous speed (CPU clock frequency or CPU clock divided by four). It is set up in conjunction with the IP Clock Speed Select Register to set the required IP frequency.

Bit 2: **SYNCX: IP Expansion Interface SYNC Clock Select.**
When CLEAR the IP expansion interface is clocked at 8 or 32MHz (dependent on the CLKX bit see above). When SET the IP expansion interface is clocked synchronously with the main CPU clock at either the CPU clock frequency or CPU clock divided by 4 (again dependent on the CLKX bit).

After RESET this bit is CLEAR (i.e. 8/32MHz clock selected).

Bit 1: **SYNCB: IP B SYNC Clock Select.**
When CLEAR IP B is clocked at 8 or 32MHz (dependent on the CLKB bit see above). When SET the IP expansion interface is clocked synchronously with the main CPU clock at either the CPU clock frequency or CPU clock divided by 4 (again dependent on the CLKB bit).

After RESET this bit is CLEAR (i.e. 8/32MHz clock selected).

Bit 0: **SYNCA: IP A SYNC Clock Select.**
When CLEAR IP A is clocked at 8 or 32MHz (dependent on the CLKA bit see above). When SET the IP expansion interface is clocked synchronously with the main CPU clock at either the CPU clock frequency or CPU clock divided by 4 (again dependent on the CLKA bit).

After RESET this bit is CLEAR (i.e. 8/32MHz clock selected).

7.10 VMEbus Slave Access Controller

7.10.1 Overview

The BVME4000/6000 allows other VMEbus masters to access some of its onboard address space. It allows accesses via either A24 or A32 address spaces. The BVME4000/6000 also acts as a location monitor for A16 accesses.

7.10.2 Standard (A24) & Extended (A32) Accesses

Both the size of the window and the base address of the window (from the VMEbus master's point of view) are programmable. The base address of the access from the onboard memory's point of view is also programmable.

Thus the BVME4000/6000 can be set-up to 'dual map' a programmable amount of memory (64Kbyte to 4Gbyte) onto the VMEbus. The local base address of the memory is programmable (on window size boundaries). The address that the 'dual mapped' memory appears at on VMEbus is also independently programmable. So, for example, 512Kbytes of memory module memory located at 00380000 could be accessed by another VMEbus master accessing location 00C00000-00C80000.

The address decoding for A24 and A32 accesses are separate from each other. There are two decoders, one for A24 and one for A32. They both work by comparing the most significant byte of the address with the programmed base address. Thus A24 space is programmable on 64Kbyte (2^{16}) boundaries, and the A32 space is programmable on 16Mbyte (2^{24}) boundaries.

The window sizing operates by masking out address bits to the comparator. Thus for A24 space the smallest window size (when no bits are masked) is 64Kbyte and for A32 is 16Mbyte. The window sizes available are powers of two up to the maximum window size of the address space (A24 = 8Mbytes, A32 = 512Mbytes).

A restriction on the window base address is that it must be on a window size boundary. Thus if the window size is 128Kbytes, the window base address must be on a 128Kbyte boundary, e.g. 00000000, 00020000, 00040000, 00D00000 etc.

The BVME4000/6000 responds to the following A24 Address Modifiers (AM) codes:

CPU Supervisor	Program Access	=	$3E
	Data Access	=	$3D
CPU User	Program Access	=	$3A
	Data Access	=	$39

The BVME4000/6000 responds to the following A32 Address Modifiers (AM) codes:

CPU Supervisor	Program Access	=	$0E
	Data Access	=	$0D
CPU User	Program Access	=	$0A
	Data Access	=	$09

7.10.3 Short I/O (A16) Accesses

The BVME4000/6000 will respond to Short I/O (A16) accesses. The size of the window is fixed at 256bytes. The base address is programmable on 256byte boundaries.

Short I/O space accesses act as a location monitor only and do not access physical memory within the BVME4000/6000. This space is used to allow 'mail box' interrupts to the processor on the BVME4000/6000. This allows other bus masters to use semaphore control with the BVME4000/6000 without the use of the VMEbus IRQ lines.

The BVME4000/6000 responds to the following A16 Address Modifiers (AM) codes:

CPU Supervisor	Data Access	=	$2D
CPU User	Data Access	=	$29

7.10.4 Controlling The Window Size

The table below shows window sizes for valid combinations of the Mask Register:

Mask Register	A24 Address Space Window Size	A32 Address Space Window Size
00	64Kb	16Mb
01	128kb	32Mb
03	256kb	64Mb
07	512Kb	128Mb
0F	1024Kb	256Mb
1F	2048Kb	512Mb
3F	4096Kb	1024Mb
7F	8192Kb	2048Mb
FF	16384Kb	4096Mb

7.10.5 Local Address Generation

The two Local Base Address registers (A32LBA and A24LBA) contain the base address of the 'dual mapped' memory window.

For A32 accesses, the unmasked (see A32MSK register description) A32 Local Base Address (A32LBA) Register bits are used as the most significant address lines during the VMEbus slave access to the onboard memory. All other local address lines are driven from the VMEbus Address bus.

For A24 accesses, The most significant eight local address lines are driven by the **A32LBA** register. The unmasked (see A24MSK register description) A24 Local Base Address (A24LBA) Register bits are used as the next most significant address lines during the VMEbus slave access to the onboard memory. All other local address lines are driven from the VMEbus Address bus.

Thus for standard (A24) VMEbus accesses both the A32LBA and the A24LBA registers need to be set up.

7.10.6 Address Control Registers

Slave accesses are controlled by eight byte wide registers. All registers are write only.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF400003	A32VBA	A31cmp	A30cmp	A29cmp	A28cmp	A27cmp	A26cmp	A25cmp	A24cmp
FF410003	A32MSK	A31msk	A30msk	A29msk	A28msk	A27msk	A26msk	A25msk	A24msk
FF420003	A24VBA	A23cmp	A22cmp	A21cmp	A20cmp	A19cmp	A18cmp	A17cmp	A16cmp
FF430003	A24MSK	A23msk	A22msk	A21msk	A20msk	A19msk	A18msk	A17msk	A16msk
FF440003	A16VBA	A15cmp	A14cmp	A13cmp	A12cmp	A11cmp	A10cmp	A9cmp	A8cmp
FF450003	A32LBA	A31ladd	A30ladd	A29ladd	A28ladd	A27ladd	A26ladd	A25ladd	A24ladd
FF460003	A24LBA	A23ladd	A22ladd	A21ladd	A20ladd	A19ladd	A18ladd	A17ladd	A16ladd
FF470003	ADDRCTL	VMELO	Rsrvd	SCVME	SCETH	A32EN	A24EN	A16EN	RAMLO

7.10.6.1 A32VBA - A32 VMEbus Base Address Register

This register contains an 8-bit value, against which extended (A32) VMEbus accesses are matched in order to determine slave access. If VMEbus A[31..24] matches, then an access to the onboard memory is performed.

7.10.6.2 A32MSK - A32 VMEbus Address Mask Register

This contains an 8-bit mask that is applied, on a bit by bit basis, to the VMEbus slave address decoding for A32 (extended) accesses from another VMEbus master. If a bit is set (a 1) then the corresponding address line is ignored. Thus the contents of this register control the size of the window decoded by the BVME4000/6000 - refer to "7.10.4 Controlling The Window Size (on page 46)" for more details.

7.10.6.3 A24VBA - A24 VMEbus Base Address Register

This contains an 8-bit value, against which standard (A24) VMEbus accesses are matched in order to determine slave access. If VMEbus A[23..16] matches, then an access to the onboard memory is performed.

7.10.6.4 A24MSK - A24 VMEbus Address Mask Register

This contains an 8-bit mask that is applied, on a bit by bit basis, to the VMEbus slave address decoding for A24 (standard) accesses from another VMEbus master. If a bit is set (a 1) then the corresponding address line is ignored. Thus the contents of this register control the size of the window decoded by the BVME4000/6000 - refer to "7.10.4 Controlling The Window Size (on page 46)" for more details.

7.10.6.5 A16VBA - A16 VMEbus Base Address Register

This contains an 8-bit value, against which A16 VMEbus accesses are matched in order to determine slave access. If VMEbus A[15..8] matches, then a Short I/O access is performed.

7.10.6.6 A32LBA - A32 Local Base Address Register

This contains an 8-bit value that is used to drive the onboard most significant address lines during an access by another VMEbus master. In other words it contains the most significant part of the local memory base address of the 'dual mapped' window - refer to "7.10.5 Local Address Generation (on page 46)" for more details.

7.10.6.7 A24LBA - A24 Local Base Address Register

This contains an 8-bit value that is used to drive the onboard next most significant address lines during an access by another VMEbus master. In other words it contains the next most significant part of the local memory base address of the 'dual mapped' window - refer to "7.10.5 Local Address Generation (on page 46)" for more details.

7.10.6.8 ADDRCTL - Address Control Register

This contains some miscellaneous control bits, After RESET all bits are CLEAR.

Bit 7: **VMELO: Map VMEbus Low.**
When CLEAR accesses to the bottom 256Mbytes of the address map are confined to local memory only; accesses to non existent memory return a bus error. When SET accesses to the bottom 256Mbytes of the address map will be to local memory (or memory module if fitted) OR to VMEbus A32:D32 address space if there is no local memory at that address.

Bit 6: **Reserved.**
For future compatibility this must be always written as zero.

Bit 5: **SCVME: VMEbus Snoop Control.**
This bit enables snooping for VMEbus Slave Accesses. When SET VMEbus slave accesses are snooped by the CPU, so that the CPU will sink and source dirty data - refer to "Appendix B CPU Cache Coherency and Bus Snooping (on page 62)" for a discussion on snooping and cache coherency.

Bit 4: **SCETH: Ethernet Snoop Control.**
This bit enables snooping for Ethernet Controller Master Accesses. When SET Ethernet Controller master accesses are snooped by the CPU, so that the CPU will sink and source dirty data - refer to "Appendix B CPU Cache Coherency and Bus Snooping (on page 62)" for a discussion on snooping and cache coherency.

Bit 3: **A32EN: VMEbus A32 Slave Access Enable.**
When SET VMEbus A32 slave accesses are enabled as specified by the A32VBA, A32MSK & A32LBA registers. When CLEAR VMEbus A32 slave accesses are disabled.

Bit 2: **A24EN: VMEbus A24 Slave Access Enable.**
When SET VMEbus A24 slave accesses are enabled as specified by the A24VBA, A24MSK, A24LBA & A32LBA registers. When CLEAR VMEbus A24 slave accesses are disabled.

Bit 1: **A16EN: VMEbus A16 Slave Access Enable.**
When SET VMEbus A16 slave accesses are enabled as specified by the A16LBA register. When CLEAR VMEbus A16 slave accesses are disabled.

Bit 0: **RAMLO: Map RAM Low.**
When SET the SRAM (located at E9000000 and F9000000) is also mapped at 00000000. This is mainly intended to provide a common address map for systems with no memory module fitted.

7.11 Configuration Switch

This is a bank of four switches that are available through the front panel. The switches have no dedicated hardware function. They are provided to allow configuration selection within software applications. The state of each switch can be read in the Configuration Switch Register.

7.11.1 Configuration Switch Layout

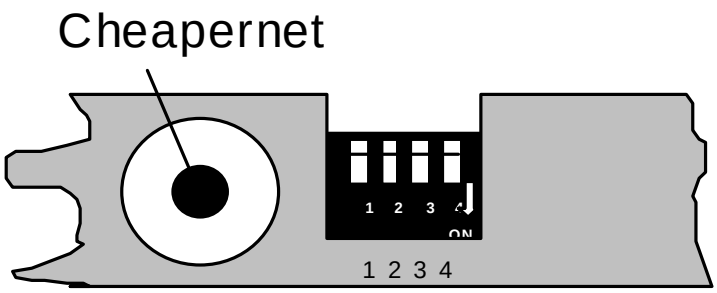


Figure 27 Configuration Switch Layout

7.11.2 Configuration Switch Register

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF500003	CONFSW	Rsrvd	Rsrvd	Rsrvd	Rsrvd	SW1	SW2	SW3	SW4

Bit 7-4: **Reserved.**
These bits are unused. When read, their state is undefined.

Bit 3-0: **SW1, SW2, SW3, SW4.**
Reflects the state of each numbered switch. When the switch is ON (lower position) the associated bit is read as ZERO. When switch is OFF (upper position) the associated bit is read as ONE.

7.12 Real Time Clock/Timers

7.12.1 Overview

The Real Time Clock and Timer facilities on the BVME4000/6000 are provided by the DP8570A Timer Clock Peripheral, which provides two 16-bit timer/counters, calendar/clock, a flexible interrupt scheme and 44 bytes of non-volatile RAM.

Two independent, multi-mode, 16 bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 8 possible clock sources. Thus, by programming the input clocks and the timer counter values a very wide range of time duration's can be achieved. The range is from 200nS (8MHz external clock) to 65,535 seconds (18hrs., 12min.).

A very flexible and powerful on-chip interrupt structure is provided. Three basic types of interrupts are available: Periodic (from 1mS to 1 minute), Alarm/Compare (from the RTC) and Timer. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

For full programming details, refer to the DP8570A documentation detailed in the "A.5 DP8570A (on page 60)" section of this manual.

7.12.2 Hardware Specific Considerations

INTR pin Configuration

The INTR pin is fed to the Interrupt Controller - refer to "7.8 Interrupt Controller (on page 35)" for more details. It must be programmed as an active low, push-pull output. This is set up in the OUTPUT MODE REGISTER by programming bit 2 (INTR Active Hi/Low) CLEAR and bit 3 (INTR Push-pull/Open Drain) SET.

T1 pin Configuration

The T1 pin (timer 1 output) is fed to the TIN pin of the PI/T (MC68230) - refer to "7.13 Parallel Port/Timer (on page 52)" for more details. It must be programmed as a push-pull output. The output may be programmed as active high or low as the application requires. This is set up in the OUTPUT MODE REGISTER by programming bit 1 (T1 Push-pull/Open Drain) SET.

MFO pin Configuration

The MFO pin is not currently connected on the BVME4000/6000.

RTC Crystal Oscillator Frequency

The BVME4000/6000 uses a 32.768 kHz crystal. This provides lowest power dissipation. The DP8570A needs to be programmed with the oscillator frequency used. This is set up in the REAL TIME MODE REGISTER by programming bits 7&6 (XT1 and XT0) both CLEAR.

TCK - External Timer Clock Input

TCK is driven from a fixed 8 MHz clock source.

PFAIL - Power Fail Input

This input is driven from the MAX791 power fail signal.

G0 & G1 - Timer Gate Inputs

These pins are pulled low on the BVME4000/6000.

7.12.3 Programming

The register map of the DP8570A is shown below. The register map consists of two 31 byte pages with a main status register that is common to both pages. A control bit (bit 7) in the Main Status Register is used to select either page. Page 0 contains all the clock and timer functions, while page 1 has non-volatile RAM.

Page 0 is further sub-divided to provide two blocks of control registers. Again a bit in the Main Status Register (bit 6) is used to select either register block.

The registers are all byte wide mapped on the least significant byte of long word boundaries.

Address	Page Select = 1	Page Select = 0	
		Register Select = 1	Register Select = 0
FF900003	Main Status Register		
FF900007	RAM	Real Time Mode	Timer 0 Control
FF90000B	RAM	Output Mode	Timer 1 Control
FF90000F	RAM	Interrupt Control 0	Periodic Flag
FF900013	RAM	Interrupt Control 1	Interrupt Routing
FF900017	RAM	$^1/_{100}$ Second Counter	
FF90001B	RAM	Seconds Clock Counter	
FF90001F	RAM	Minutes Clock Counter	
FF900023	RAM	Hours Clock Counter	
FF900027	RAM	Day of Month Clock Counter	
FF90002B	RAM	Months Clock Counter	
FF90002F	RAM	Years Clock Counter	
FF900033	RAM	Units Julian Clock Counter	
FF900037	RAM	100s Julian Clock Counter	
FF90003B	RAM	Day of Week Clock Counter	
FF90003F	RAM	Timer 0 LSB	
FF900043	RAM	Timer 0 MSB	
FF900047	RAM	Timer 1 LSB	
FF90004B	RAM	Timer 1 MSB	
FF90004F	RAM	Seconds Compare RAM	
FF900053	RAM	Minutes Compare RAM	
FF900057	RAM	Hours Compare RAM	
FF90005B	RAM	Day of Month Compare RAM	
FF90005F	RAM	Months Compare RAM	
FF900063	RAM	Day of Week Compare RAM	
FF900067	RAM	Seconds Time Save RAM	
FF90006B	RAM	Minutes Time Save RAM	
FF90006F	RAM	Hours Time Save RAM	
FF900073	RAM	Day of Month Time Save RAM	
FF900077	RAM	Months Time Save RAM	
FF90007B	RAM	RAM	
FF90007F	RAM	RAM/TEST	

7.13 Parallel Port/Timer

7.13.1 Overview

The Parallel Interface/Timer (PI/T) is based on the MC68230. This block provides a bi-directional, 8-bit, double-buffered, Centronics compatible parallel Interface. This interface is electrically buffered to provide 48mA of drive. Connection can be made via the front panel connector JP3 or via a paddle board connected to the backplane P2.

The PI/T provides internal Board Control Register functions to control SCC clock selection, Watchdog refresh and VMEbus Arbitration Selection.

The PI/T contains an independent, 24-bit timer with a 5-bit prescaler. The timer may be clocked from the PI/T clock pin or from the T1 output pin of the RTC Timer 1 - refer to "7.12 Real Time Clock/Timers (on page 50)" for more details. It can generate periodic interrupts or a single interrupt after programmed time period. The CLK pin is driven from CPUCLK divided by 4, thus with a 25MHz bus clock, the PI/T CLK is driven at 6.25MHz.

For full programming details, refer to the MC68230 documentation detailed in the "A.7 MC68230 (on page 60)" section of this manual.

7.13.2 Port A Usage

The MC68230 port A is available for use as an 8-bit parallel I/O port. It is buffered using a bi-directional transceiver to give 48mA of drive. The direction control of the transceiver is via port C - refer to "7.13.4 Port C Usage (on page 54)" for more details. Any of the port A sub-modes may be used. However, because the port is connected to an 8-bit wide transceiver, ALL the bits must be programmed to be in the same direction; all inputs or all outputs. The direction programmed must match that of the transceiver set up via port C.

7.13.3 Port B Usage

The MC68230 port B is dedicated as an internal Board Control Register. This port needs to be configured for simple pin I/O. Therefore the MC68230 must be configured for Port Mode 0. This is set up in the PORT GENERAL CONTROL REGISTER by programming bits 7 & 6 both CLEAR. Port B must be configured to Sub Mode 1X. This is set up in the PORT B CONTROL REGISTER by programming bit 7 SET.

D7	D6	D5	D4	D3	D2	D1	D0
OUT	OUT	OUT	OUT	OUT	IN/OUT	OUT	OUT
/RRS	/SYSCON	RQLVL1	RQLVL0	SCL	SDA	SCLKA	SCLKB

Bit 7: **/RRS: Round Robin Select.**
This must be programmed as an output pin. This bit controls the VMEbus arbitration mechanism used by the BVME4000/6000 when enabled as a System Controller. When the bit is SET straight prioritised (PRI) or single level (SGL) is used. When CLEAR Round Robin Select (RRS) is used. See Section 3 of the VMEbus Specification for a full description - refer to "A.8 VMEbus (on page 60)" for details of this documentation.

Bit 6: **/SYSCON: System Controller Function Enable.**
This must be programmed as an output pin. This bit controls whether the BVME4000/6000 is the VMEbus System Controller unless overridden by the System Controller Link - refer to "5.2.12 LK22 VMEbus System Controller Enable (on page 17)" for more details. When programmed as the VMEbus System Controller, the BVME4000/6000 performs as the VMEbus arbiter, it drives VMEbus SYSCLK and VMEbus BCLR. When the bit is SET the BVME4000/6000 is NOT the System controller. When CLEAR the BVME4000/6000 is the VMEbus System Controller.

Bit 5,4: **RQLVL1,RQLVL0: VMEbus Request Level Selection.**
These must be programmed as output pins. The BVME4000/6000 can request mastership of the VMEbus on any of the four VMEbus request levels. These two bits select which level VMEbus requests are made upon:

RQLVL1	RQLVL0	VMEbus Request Level
0	0	Requests on level 0
0	1	Requests on level 1
1	0	Requests on level 2
1	1	Requests on level 3

Bit 3: **SCL: Serial Clock Line.**
This must be programmed as an output pin. This bit controls the I^2C Clock Line, used for clocking data in and out of the NM24C02 EEPROM. When the bit is SET the clock line is HIGH, when the bit is CLEAR the clock line is LOW. For full programming details, refer to the NM24C02 documentation detailed in the "A.11 NMC24C02 (on page 61)" section of this manual.

Bit 2: **SDA: Serial Data Line.**
This is the I^2C Data Line, used for reading the data to/from the NM24C02 EEPROM. When the set as an output pin, the data will be OUTPUT to the EEPROM, when set as an input pin, the data will be INPUT from the EEPROM. The bit sets the data to the EEPROM in output mode, and reflects the data from the EEPROM in input mode. For full programming details, refer to the NM24C02 documentation detailed in the "A.11 NMC24C02 (on page 61)" section of this manual.

Bit 1: **SCLKA: Serial Communications Controller Clock Select for Channel A.**
This must be programmed as an output pin. This bit controls which clock source is applied to the RTxCA pin of the SCC. Refer to "7.14 Serial Communications Controller (on page 56)" for details of Baud Rate generation for Serial channels. The clock source can be selected between an onboard crystal and an external clock from the P2 connector.

SCLKA Value	Clock Applied to RTxCA
0	Onboard Crystal - 7.3728 MHz
1	SCLKINA signal from P2 (pin 4c)

Bit 0: **SCLKB: Serial Communications Controller Clock Select for Channel B.**
This must be programmed as an output pin. This bit controls which clock source is applied to the RTxCB pin of the SCC. . Refer to "7.14 Serial Communications Controller (on page 56)" for details of Baud Rate generation for Serial channels. The clock source can be selected between an onboard crystal and an external clock from the P2 connector.

SCLKB Value	Clock Applied to RTxCB
0	Onboard Crystal - 7.3728 MHz
1	SCLKINB signal from P2 (pin 8c)

7.13.4 Port C Usage

The MC68230 port C is nominally an 8 bit general purpose I/O port (similar to Ports A & B). However five of the pins carry special functions associated with interrupts and timer operation.

The PORT SERVICE REQUEST REGISTER should be set up to use vectored interrupts on PIRQ and PIACK. Thus bits 4 & 3 should be set as: Bit 4 SET, Bit 3 SET. The PORT INTERRUPT VECTOR REGISTER should be set up with the required Interrupt vector.

The TIMER CONTROL REGISTER should be set up to use vectored interrupts on TOUT and TIACK. Thus bits 7 & 6 should be set as: Bit 7 SET, Bit 6 CLEAR. Bit 5 should be used as an interrupt enable bit. The TIMER INTERRUPT VECTOR REGISTER should be set up with the required Interrupt vector.

D7	D6	D5	D4	D3	D2	D1	D0
Special	Special	Special	IN/OUT	Special	Special	OUT	OUT
/TIACK	/PIACK	/PIRQ	WDOG	TOUT	TIN	PADIR	PAEN

Bit 7: **/TIACK: Timer Interrupt Acknowledge.**
The Interrupt Controller assumes that the MC68230 Timer Interrupter supports vectored interrupts. This pin is connected to the Interrupt Controller's TIMIACK line.

Bit 6: **/PIACK: Parallel Port Interrupt Acknowledge.**
The Interrupt Controller assumes that the MC68230 Parallel Interrupter supports vectored interrupts. This pin is connected to the Interrupt Controller's PARIACK line.

Bit 5: **/PIRQ: Parallel Port Interrupt Request.**
This output drives the 68230 Parallel Interrupt input to the Interrupt Controller - refer to "7.8 Interrupt Controller (on page 35)" for more details.

Bit 4: **WDOG: WatchDog Refresh.**
This bit drives the input to the watchdog circuit. When this bit is configured as an INPUT, the watchdog function is disabled. When configured as an OUTPUT, the watchdog is enabled and this bit must be toggled every second if a Watchdog time out is to be avoided. If the WDOG bit is not toggled within the time out period (1 second minimum) then a hardware reset will be generated.

Bit 3: **TOUT: Timer Output.**
This output drives the 68230 Timer Interrupt input to the Interrupt Controller - refer "7.8 Interrupt Controller (on page 35)" for more details.

Bit 2: **TIN: Timer Input.**
This input is driven from the T1 output of the DP8570A - refer to "7.12 Real Time Clock/Timers (on page 50)" for more details.

Bit 1: **PADIR: Port A Direction.**
This OUTPUT controls the DIRECTION of the transceiver. When SET the transceiver will drive OUT from the BVME4000/6000 to the connector. When CLEAR the transceiver will receive IN from the connector and drive into Port A.

Bit 0: **PAEN: Port A Enable.**
This OUTPUT controls the ENABLE to the transceiver. When SET the transceiver is disabled and its outputs are hi-impedance. When CLEAR the transceiver is enabled and will drive in the direction controlled by its DIRECTION input.

7.13.5 Handshake Pin Usage

H1: This must be configured as an input. It is connected to /PACKNOW signal via an inverting buffer.

H2: This must be configured as an output. It is connected to /PSTROBE signal via an inverting buffer.

H3: This must be configured as an input. It is connected to PBUSY signal via an inverting buffer.

H4: This signal is currently not connected on the BVME4000/6000.

7.13.6 MC68230 PI/T Registers

The register map of the MC68230 is shown below. The register map consists of a bank of 32 byte wide registers (of which some are undefined). The registers are mapped on the least significant byte of long words.

Address	Register	Access	Affected by Reset	Affected by Access
FFA00003	Port General Control Register	R/W	Yes	No
FFA00007	Port Service Request Register	R/W	Yes	No
FFA0000B	Port A Data Direction Register	R/W	Yes	No
FFA0000F	Port B Data Direction Register	R/W	Yes	No
FFA00013	Port C Data Direction Register	R/W	Yes	No
FFA00017	Port Interrupt Vector Register	R/W	Yes	No
FFA0001B	Port A Control Register	R/W	Yes	No
FFA0001F	Port B Control Register	R/W	Yes	No
FFA00023	Port A Data Register	R/W	No	Yes
FFA00027	Port B Data Register	R/W	No	Yes
FFA0002B	Port A Alternate Register	R	No	No
FFA0002F	Port B Alternate Register	R	No	No
FFA00033	Port C Data Register	R/W	No	No
FFA00037	Port Status Register	R/W	Yes	No
FFA0003B	Reserved			
FFA0003F	Reserved			
FFA00043	Timer Control Register	R/W	Yes	No
FFA00047	Timer Interrupt Vector Register	R/W	Yes	No
FFA0004B	Reserved			
FFA0004F	Counter Preload Register High	R/W	No	No
FFA00053	Counter Preload Register Middle	R/W	No	No
FFA00057	Counter Preload Register Low	R/W	No	No
FFA0005B	Reserved			
FFA0005F	Counter Register High	R	No	No
FFA00063	Counter Register Middle	R	No	No
FFA00067	Counter Register Low	R	No	No
FFA0006B	Timer Status Register	R/W	Yes	No
FFA0006F	Reserved			

7.14 Serial Communications Controller

7.14.1 Overview

The Serial Communications Controller (SCC) resource is based on the Z85230. This block provides two independent, full-duplex serial communication channels. Both channels handle asynchronous, byte synchronous and bit synchronous protocols. Each channel has its own baud rate generator, clocked from a variety of sources, including a Digital Phase Locked Loop (DPLL).

Each channel can be independently electrically buffered as RS232, RS422 or RS485. Connection can be made via the front panel connectors JP1 and JP2 or via a paddle board connected via the P2 connector.

For full programming details, refer to the Z85230 documentation detailed in the "A.6 Z85230 (on page 60)" section of this manual.

7.14.2 Serial Clock Sources

PCLK This is the master Z85230 clock pin. It is used to synchronise all internal signals. It is available as a clock source to the baud rate generator. The BVME4000/6000 drives this signal with the processor clock divided by 2. Thus with a 25MHz bus clock, the Z85230 is clocked at 12.5MHz. Because this pin is CPU clock dependent it is recommended that it is not used for baud rate generation.

RTxCA This input pin can be programmed to supply any combination of: the receive clock, the transmit clock, the baud rate generator and the DPLL. The BVME4000/6000 drives this signal from a multiplexer controlled by the SCLKA bit of the BOARD CONTROL REGISTER. Refer to "7.13 Parallel Port/Timer (on page 52)" for more details of this register. The clock source can be selected between an onboard 7.3728MHz crystal and an external clock from P2 Connector.

SCLKA Value	Clock Applied to RTxCA
0	Onboard Crystal - 7.3728 MHz
1	SCLKINA signal from P2 (pin 4c)

RTxCB This input pin can be programmed to supply any combination of: the receive clock, the transmit clock, the baud rate generator and the DPLL. The BVME4000/6000 drives this signal from a multiplexer controlled by the SCLKB bit of the BOARD CONTROL REGISTER. Refer to "7.13 Parallel Port/Timer (on page 52)" for more details of this register. The clock source can be selected between an onboard 7.3728MHz crystal and an external clock from P2 Connector.

SCLKB Value	Clock Applied to RTxCB
0	Onboard Crystal - 7.3728 MHz
1	SCLKINB signal from P2 (pin 8c)

TRxCA This pin is connected to the SCLKOUTA signal on P2 pin 4a. It can be programmed to be either an input or an output. When programmed as an input, a clock source is received and can then supply the clock to the receiver and/or the transmitter. When programmed as an output, it can supply a clock from; the RTxCA pin, the RxDPLL or the baud rate generator.

TRxCB This pin is connected to the SCLKOUTB signal on P2 pin 8a. It can be programmed to be either an input or an output. When programmed as an input, a clock source is received and can then supply the clock to the receiver and/or the transmitter. When programmed as an output, it can supply a clock from; the RTxCB pin, the RxDPLL or the baud rate generator.

7.14.3 Programming

Each channel has a data register, when it is read, the receiver FIFO is read. When it is written, the transmitter FIFO is written.

Each channel also has a number of Write Registers and Read Registers that are used to control the operation of the channel. These are generally accessed as a two step procedure. First the register to be accessed is written to the Control Register, then the next access to the Control Register accesses the referenced Read or Write Register.

Address	Register Access
FFB00003	Control Register - Channel B (JP2)
FFB00007	Data Register - Channel B (JP2)
FFB0000B	Control Register - Channel A (JP1)
FFB0000F	Data Register - Channel A (JP1)

The BVME4000/6000 supports vectored interrupts from the SCC - refer to "7.8 Interrupt Controller (on page 35)" for more details.

8. Specifications

8.1 On-Board Functions

BVME4000: MC68040, MC68LC040 or MC68EC040 CPU at 25MHz/33MHz.
BVME6000: MC68060, MC68LC060 or MC68EC060 CPU at 50MHz/66MHz (25MHz/33MHz bus).

Z85230 Dual Serial interface controller, 7.3728MHz or external clock source,
RS232 buffers (RS422 & RS485 options), front panel and P2 connections.
DP8570A Timer Clock Peripheral (calendar-clock, 3 timers, 44 byte NVR).
MC68230 Parallel Interface/Timer, front panel and P2 printer connections.
NCR53C710-1 DMA SCSI Controller, header and P2 connections.
85296CA DMA Ethernet/Cheapernet Controller,
Front panel BNC Cheapernet and P2 AUI connections (RJ45 10BaseT option).
MAX791 Watchdog: refresh period = 1000mS (when enabled).

2 x 32-pin CPU PROM sockets, 16-bit wide, accept 512Kbit to 8Mbit EPROM's, 4Mbit FLASH,
(90ns @ 25MHz bus, 120ns @ 33MHz bus).
512K/2Mbytes CMOS SRAM, 32-bit wide, battery backed (up to 7 days or 2.5 years).
32-bit wide memory module interface with burst-fill up to 2/1/1/1.
2Kbit serial access EEPROM.
LOCAL BUS TIMEOUT period 64 CPU clocks (2.56µS @ 25MHz bus clock).

RED LED indicates VMEbus MASTER access.
GREEN LED indicates processor status.

RESET switch (if enabled).
ABORT switch (level 7 auto-vectored interrupt).

8.2 VMEbus Master

FAIR Bus Requester, request on any of 4 levels.
A32, A24, A16
D32, D16, D08(EO)
RMW
AM6

8.3 VMEbus Slave

A32, A24, A16
D32, D16, D08(EO)
RMW
AM6
LOCATION MONITOR

8.4 VMEbus System Controller Functions

ARBITER: SGL, PRI or RRS, software programmable, FAIR ROR (RWD option).
SYSCLK Driver.
SYSRESET Driver/Monitor power-up and switch.
VMEbus RESET minimum period = 200mS.
BUS TIMEOUT period 128µS.
BUS ERROR monitor.
ACFAIL monitor (level 7 auto-vectored interrupt).

8.5 VMEbus Interrupts

Interrupter D08(O) ROAK:
I(1-7) single level, software programmable;
Interrupt vector ID, software programmable.

Interrupt handler D08(O): I(1-7) all levels, software maskable.

8.6 IP Functions

Two IP compatible sites:
2 x Single IPs (16-bit) or 1 x Double IP (32-bit);
8MHz, 32MHz or CPU synchronous IP clocks, software selectable;
Software programmable IP interrupts;
Front panel IP I/O connections.

IP expansion connector:
Supports up to four additional IP compatible sites.

8.7 Board Configuration

Configuration Switch: 4-bit, software readable.

LINKS:
ABORT/RESET switch enable;
VMEbus RESET IN/OUT enable;
VMEbus SYSTEM CONTROLLER enable;
CPU cache inhibit;
Cheapernet Heartbeat enable;
Cheapernet/Ethernet select;
PROM type;
SCSI Termination select;
SRAM backup source select.

PROGRAM: VMEbus SYSTEM CONTROLLER functions;
VMEbus Master Request Level;
VMEbus SLAVE addressing;
VMEbus interrupt handler levels;
VMEbus interrupt level & vector ID;
Local SRAM & VMEbus mapping;
IP interrupt levels;
IP clock sources;
Serial Port clock sources.

8.8 Operating Environment

Dimensions: 160mm x 233.35mm (6U) single slot.

Power:

+5V	+0.25V/-0.125V	<50mV noise/ripple	2.2A typical;
+12V	+0.60V/-0.36V	<50mV noise/ripple	150mA maximum;
-12V	-0.60V/+0.36V	<50mV noise/ripple	0mA;

RESET @ <4.65V, RTC disable @ <4.8V.
Note: power requirements exclude IP, Memory Module & Disc Drive power.

Environmental: 0 to 70 °C, 95% humidity non-condensing (extended range to order).
Refer to "Appendix E Thermal Management (on page 68)" for airflow/heatsink requirements.

Appendix A Data Sheet & Manual References

A.1 MC68040/68LC040/68EC040 User's Manual

MOTOROLA MC68040 MC68EC040 MC68LC040 MICROPROCESSORS USER'S MANUAL (1992, MOTOROLA order number: M68040UM/AD).

MOTOROLA PROGRAMMER'S REFERENCE MANUAL (1991, MOTOROLA order number: M68000PM/AD).

A.2 MC68060/68LC060/68EC060 User's Manual

MOTOROLA MC68060 MC68LC060 MC68EC060 MICROPROCESSORS USER'S MANUAL (1994, MOTOROLA order number: M68060UM/AD).

MOTOROLA PROGRAMMER'S REFERENCE MANUAL (1991, MOTOROLA order number: M68000PM/AD).

A.3 82596CA User's Manual

INTEL 32-Bit Local Area Network (LAN) Compliant User's manual (1992, INTEL order number: 296853-001).

INTEL 82596CA HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR DATA SHEET (July 1992, INTEL order number: 290218-005).

A.4 53C710 Data Manual & Programmers Guide

NCR53C710, 53C710-1 SCSI I/O Processor Data Manual (June 1992, NCR Corporation).

NCR53C710 SCSI I/O Processor Programmers Guide (Sept 1990, NCR Corporation)

A.5 DP8570A Data Sheet

NATIONAL SEMICONDUCTOR DP8570A Timer Counter Peripheral (TCP) Data Sheet (May 1993, TL/F/8638).

A.6 Z85230 User's Manual

ZILOG SCC User's Manual (Q4/1992).

A.7 MC68230 Data Sheet

MOTOROLA MC68230 PARALLEL INTERFACE/TIMER (PI/T) Data Sheet (Dec 1983).

A.8 VMEbus Specification

THE VMEbus SPECIFICATION (Sept 1987, VITA).

A.9 RS422/485 Interface Module User's Manual

BVM 453-62370/62371 RS422/RS485 INTERFACE MODULE User's Manual (BVM part number: 454-68370).

A.10 AM29F040 Data Book

AMD Flash Memory Products Data Book/Handbook 1996.

A.11 NMC24C02 Data Sheet

NATIONAL SEMICONDUCTOR NMC24Cxx – Standard 2-Wire Bus Interface Serial EEPROM Family (May 1996).

A.12 MEM390 Memory Module User's Manual

MEM390 4/8 Mbyte DRAM MEMORY MODULE User's Manual (BVM part number: 454-68391).

A.13 MEM400 Memory Module User's Manual

MEM400 16Mbytes DRAM 4/8 Mbytes FLASH MEMORY MODULE User's Manual (BVM part number: 454-61400).

A.14 MEM480 Memory Module User's Guide

MEM480 16/32/48Mbytes DRAM MEMORY MODULE User's Guide (BVM part number: 454-61480).

A.15 MEM4SD Memory Module User's Guide

MEM4SD 16 to 512Mbytes SDRAM MEMORY MODULE User's Guide (BVM part number: 454-61490).

A.16 EXP100 Quad IP Expansion User's Manual

EXP100 Quad IP Expansion User's Manual (BVM part number: 454-44100).

Appendix B CPU Cache Coherency and Bus Snooping

B.1 BVME4000 (MC68040)

The MC68040 is a third generation 68000 series processor with separate data and instruction caches of 4Kbytes each. The cache unit supports full copyback caching, in addition to write-through caching (as available on earlier processors), cache inhibited, and bus-serialised cache modes.

Copyback caching means that when data is written out by the program, it may only reach the cache, and not the main memory. This poses cache coherency problems over those normally associated with earlier 68000 series processors (e.g. 68030), as the main memory can contain stale data, affecting DMA operations transferring data from dual-ported memory as well as to dual ported memory.

Bus serialisation is required as the 68040's internal architecture has a high degree of parallelism. Reads and writes do not occur in the order in which they are defined by the programmer. Normally this causes no problem as the 68040 will detect any clashes and synchronise them, but if accesses are being made to I/O areas for example, the ordering of reads and writes are very important. Bus serialised regions cause correct ordering of the reads and writes.

It follows on from the above that it is important to be able to define regions of the address space as operating in different caching modes. This isn't strictly a caching issue, but is very relevant to the operation of system and user software.

Use is made of the 68040's "Transparent Translation Registers" and MMU "Page Tables" to define the caching mode for different regions of the address space. The 68LC040 also has an MMU, and functions exactly the same way as a 68040 in this respect. On the 68EC040 however, although the MMU is not available, the Transparent Translation Registers are still present, and can be used for this function, although the strategy needs to be slightly different.

The 68040's Transparent Translation Registers contain an address and mask field to allow definition of an address range to be used. They also contain fields to specify the relevant caching modes for the defined region. There are four registers, two for data DTT0 and DTT1 and two for instructions ITT0 and ITT1.

The TT0 registers override the TT1 registers if there is any overlap, and undefined regions will be accessed in the 68040's default mode (write-through caching enabled) if the MMU is disabled. If the MMU is enabled (not on 68EC040) any regions undefined in the TT registers will be checked in the Page Tables. The Page Tables relate to a 4 or 8KByte region, and the caching mode is specified in a field of the page descriptor in a similar way to the TT registers.

On the BVME4000 with a 68040 or 68LC040 processor, a cache-inhibited, bus-serialised region can be defined from $F0000000 to $FFFFFFFF for access to IP Memory, EPROM, SRAM, VMEbus A24, VMEbus A16 & on-board registers for supervisor access. The rest of the address space is defined as write-through caching for instructions and copy-back caching for data for supervisor mode. The page descriptors would be used to define the regions for user-state accesses, allocated on a dynamic basis (by operating system software). The values that need to be set into the 68040 TT registers to implement this scheme are as follows:

DTT0 = $F00FA040, DTT1 = $00FFA020, ITT0 = NOT USED, ITT1 = $00FFA000

On the BVME4000 with a 68EC040 processor, a similar scheme as that for the 68040/68LC040 can be set up. This gives an I/O region from $F0000000 to $FFFFFFFF for supervisor and user-state access, with the rest of the address space defined as write-through caching for instructions and copyback caching for data for supervisor and user-state access. The values that need to be set into the 68EC040 TT registers to implement this scheme are as follows:

DTT0 = $F00FC040, DTT1 = $00FFC020,ITT0 = NOT USED, ITT1=$00FFC000

Note that instruction caching only functions in write-through mode, not copy-back mode, as no writes occur to the instruction address space. To use write-through caching in place of copyback, the "$20" should be replaced by a "$00" in the above values for DTT1.

The DTT1 and ITT1 values could be changed to introduce a third region of write-through caching in addition to copy-back caching as follows for the 68EC040:

DTT1 = $000FC020, ITT1 = $000FC000

Now the on-board RAM is defined as copy-back caching from $00000000 to $0FFFFFFF and the region from $10000000 to $EFFFFFFF is defined as write-through caching (the 68EC040's default). A similar mechanism may be used via the page descriptors when the MMU is used in the 68040 or 68LC040.

It is useful to have different regions defined for the same address space, because as the BVME4000 dual-maps some of the address space, it can be accessed in different caching modes. If the above scheme was adopted, then the VMEbus A24 space could be accessed at address $EE000000 as write-through cached, and at address $FE000000 as cache-inhibited bus-serialised access.

The BVME4000 has three separate blocks capable of bus mastership (DMA) other than the processor itself: the Ethernet Controller, SCSI Controller and the VMEbus Slave Interface. When any of these bus masters transfer data directly into a memory region (DMA), cache coherency problems can occur, as the processor may not know that data in it's internal caches is now invalid.

This problem can be approached in a number ways:

1. Normally main system memory resides on the BVME4000, and the 68040 can use "bus-snooping" to monitor accesses to the memory by any of the other bus masters. The bus-snooping must be enabled by programming the relevant bus-snoop enable bit(s) for the bus master in question. For the Ethernet Controller and VMEbus Slave Interface, there is a SNOOP ENABLE bit - refer to "7.10 VMEbus Slave Access Controller (on page 45)" for more details. For the SCSI Controller, there are SNOOP MODE bits in it's register set - refer to the 53C710 documentation detailed in the "A.4 53C710 Data Manual & Programmers Guide (on page 60)" section of this manual.

2. The 68040's internal caches can be "flushed" if it is known that their data may be invalid (e.g. when an interrupt occurs after a DMA operation). It may also be necessary to do a "cache push" if copyback caching is in use. This can be very wasteful, as data not involved in the transfers at all will also be purged from the caches.

3. Non-cached regions can be used to access the memory. For example, the Ethernet Controller can be set-up to DMA into a separate buffer region (e.g. the SRAM), which is accessed via a non-cached address. In this case, bus-snooping is not required, but the data, once DMAed into memory, is not subject to the advantages of caching. This does also have a potential performance advantage, as there is a timing overhead involved in bus-snooping by the 68040 processor.

Other schemes may be determined by the user, or a combination of the above may be used in conjunction.

B.2 BVME6000 (MC68060)

The MC68060 is a superscaler 68000 series processor with separate data and instruction caches of 8Kbytes each. The cache unit supports full copyback caching, in addition to write-through caching (as available on earlier processors), cache-inhibited imprecise-mode and precise-mode (bus-serialised) cache modes.

Copyback caching means that when data is written out by the program, it may only reach the cache, and not the main memory. This poses cache coherency problems over those normally associated with earlier 68000 series processors (e.g. 68030), as the main memory can contain stale data, affecting DMA operations transferring data from dual-ported memory as well as to dual ported memory.

Cache-inhibited precise-mode is required as the 68060's internal architecture has a high degree of parallelism. Reads and writes do not occur in the order in which they are defined by the programmer. Normally this causes no problem as the 68060 will detect any clashes and synchronise them, but if accesses are being made to I/O areas for example, the ordering of reads and writes are very important. Cache-inhibited precise-mode regions cause correct ordering of the reads and writes.

It follows on from the above that it is important to be able to define regions of the address space as operating in different caching modes. This isn't strictly a caching issue, but is very relevant to the operation of system and user software.

Use is made of the 68060's "Transparent Translation Registers" and MMU "Page Tables" to define the caching mode for different regions of the address space. The 68LC060 also has an MMU, and functions exactly the same way as a 68060 in this respect. On the 68EC060 however, although the MMU is not available, the Transparent Translation Registers are still present, and can be used for this function, although the strategy needs to be slightly different.

The 68060's Transparent Translation Registers contain an address and mask field to allow definition of an address range to be used. They also contain fields to specify the relevant caching modes for the defined region. There are four registers, two for data DTT0 and DTT1 and two for instructions ITT0 and ITT1.

The TT0 registers override the TT1 registers if there is any overlap, and undefined regions will be accessed in the 68060's default mode set in the "Translation Control Register" TCR (normally write-through caching enabled) if the MMU is disabled. If the MMU is enabled (not on 68EC060) any regions undefined in the TT registers will be checked in the Page Tables. The Page Tables relate to a 4 or 8KByte region, and the caching mode is specified in a field of the page descriptor in a similar way to the TT registers.

On the BVME6000 with a 68060 or 68LC060 processor, a cache-inhibited, precise-mode region can be defined from $F0000000 to $FFFFFFFF for access to IP Memory, EPROM, SRAM, VMEbus A24, VMEbus A16 & on-board registers for supervisor access. The rest of the address space is defined as write-through caching for instructions and supervisor data access. The page descriptors would be used to define the regions for user-state accesses including copyback regions, allocated on a dynamic basis (by operating system software). The values that need to be set into the 68060 TT registers to implement this scheme are as follows:

DTT0 = $F00FA040, DTT1 = $00FFA000, ITT0 = NOT USED, ITT1 = $00FFA000

On the BVME6000 with a 68EC060 processor, a similar scheme as that for the 68060/68LC060 can be set up. This gives an I/O region from $F0000000 to $FFFFFFFF for supervisor and user-state access, with the rest of the address space defined as write-through caching for instructions and supervisor data, and copyback caching for user-state data access. The values that need to be set into the 68EC060 TT registers to implement this scheme are as follows:

DTT0 = $F00FC040, DTT1 = $00FFC020,ITT0 = NOT USED, ITT1=$00FFC000

Note that instruction caching only functions in write-through mode, not copy-back mode, as no writes occur to the instruction address space. To use write-through caching in place of copyback, the "$20" should be replaced by a "$00" in the above values for DTT1.

The DTT1 and ITT1 values could be changed to introduce a third region of write-through caching in addition to copy-back caching as follows for the 68EC060:

DTT1 = $000FC020, ITT1 = $000FC000

Now the on-board RAM is defined as copy-back caching from $00000000 to $0FFFFFFF and the region from $10000000 to $EFFFFFFF is defined as default caching set in the TCR (normally write-through caching enabled). A similar mechanism may be used via the page descriptors when the MMU is used in the 68060 or 68LC060.

It is useful to have different regions defined for the same address space, because as the BVME6000 dual-maps some of the address space, it can be accessed in different caching modes. If the above scheme was adopted, then the VMEbus A24 space could be accessed at address $EE000000 as write-through cached, and at address $FE000000 as cache-inhibited precise-mode access.

The BVME6000 has three separate blocks capable of bus mastership (DMA) other than the processor itself: the Ethernet Controller, SCSI Controller and the VMEbus Slave Interface. When any of these bus masters transfer data directly into a memory region (DMA), cache coherency problems can occur, as the processor may not know that data in it's internal caches is now invalid.

This problem can be approached in a number ways:

1. Normally main system memory resides on the BVME6000, and the 68060 can use "bus-snooping" to monitor accesses to the memory by any of the other bus masters. The bus-snooping must be enabled by programming the relevant bus-snoop enable bit(s) for the bus master in question. For the Ethernet Controller and VMEbus Slave Interface, there is a SNOOP ENABLE bit - refer "7.10 VMEbus Slave Access Controller (on page 45)" for more details. For the SCSI Controller, there is the SC0 SNOOP MODE bit in it's register set - refer to the 53C710 documentation detailed in the "A.4 53C710 Data Manual & Programmers Guide (on page 60)" section of this manual. The memory must be accessed in write-through caching mode as the 68060 can only invalidate cache entries, unlike the 68040 which can source and sink data from/to the cache. This means that supervisor accesses (i.e. operating system software) are write-through, whereas user-state accesses would normally be copyback.

2. The 68060's internal caches can be "flushed" if it is known that their data may be invalid (e.g. when an interrupt occurs after a DMA operation). It may also be necessary to do a "cache push" if copyback caching is in use. This can be very wasteful, as data not involved in the transfers at all will also be purged from the caches.

3. Non-cached regions can be used to access the memory. For example, the Ethernet Controller can be set-up to DMA into a separate buffer region (e.g. the SRAM), which is accessed via a non-cached address. In this case, bus-snooping is not required, but the data, once DMAed into memory, is not subject to the advantages of caching. This does also have a potential performance advantage, as there is a timing overhead involved in bus-snooping by the 68060 processor.

Other schemes may be determined by the user, or a combination of the above may be used in conjunction.

Appendix C Memory Module Pinout

M 1			M 2			M 3		
PIN	Name	Function	PIN	Name	Function	PIN	Name	Function
1	A31		1	/RST	Reset Module	1	D0	
2	A30		2	TT1	Transfer	2	D1	
3	A29		3	TT0	Type #	3	D2	
4	A28		4	TM2	Transfer	4	D3	
5	A27		5	TM1	Modifier#	5	D4	
6	A26		6	TM0		6	D5	
7	A25		7	+5V	5 Volt Power	7	D6	
8	A24		8	/WE	Write Enable #	8	D7	
9	A23	A	9	SIZ1	Transfer	9	D8	
10	A22	D	10	SIZ0	Size #	10	D9	D
11	A21	D	11	GND	Ground	11	D10	A
12	A20	R	12	/TS	Transfer Start #	12	D11	T
13	A19	E	13	/TIP	Trans. In Prog. #	13	D12	A
14	A18	S	14	/LOCK	Locked (RMW) #	14	D13	
15	A17	S	15	+5V	5 Volt Power	15	D14	L
16	A16		16	/TA	Transfer Ack. #	16	D15	I
17	A15	L	17	SC1	Snoop	17	D16	N
18	A14	I	18	SC0	Control #	18	D17	E
19	A13	N	19	GND	Ground	19	D18	S
20	A12	E	20	CLK	CPU Clock #	20	D19	
21	A11	S	21	GND	Ground	21	D20	#
22	A10		22	/MIRQ	Module IRQ	22	D21	
23	A9	#	23	/MI	Memory Inhibit #	23	D22	
24	A8		24	+5V	5 Volt Power	24	D23	
25	A7		25	GND	Ground	25	D24	
26	A6		26	CLK2	CPU Clock2 #	26	D25	
27	A5		27	GND	Ground	27	D26	
28	A4		28	MERR	Module Error	28	D27	
29	A3		29	N/C	No Connect	29	D28	
30	A2		30	GND	Ground	30	D29	
31	A1		31	+5VSB	5V Standby Power	31	D30	
32	A0		32	+12V	12 Volt Power	32	D31	

NOTES: This allows connection to a BVM Memory Module. # indicates a direct connection to the equivalent processor signal, see the MC68040 and MC68060 manual or data sheet for an explanation. /RST is a general reset signal, /MIRQ is an interrupt signal from the module, and MERR is a bus error signal from the module. The 12 volt power connection is not switched, and is intended for FLASH memory programming on those modules that support it. The 5 volt standby power supply is connected directly to the VMEbus +5STDBY line, and is intended for non-volatile SRAM backup on those modules that support it.

The interface is not intended for user connection, the pinout is provided here for reference only.

Some memory modules provide a JTAG programming strip to allow direct programming from the host module. This connector detail is known as M4, the connections are shown below, and are **for factory use only**.

M4			
PIN	Name	PIN	Name
1	TCK	6	Vcc
2	GND	7	TDO
3	TMS	8	GND
4	GND	9	TRST
5	TDI	10	ENABLE

Appendix D IP Expansion Interface Pinout

J3 Pin	Row a	Row b
1	GND	GND
2	/WE	/RESET
3	D16	D17
4	D18	D19
5	D20	D21
6	D22	D23
7	D24	D25
8	D26	D27
9	D28	D29
10	D30	D31
11	/BS0	/BS1
12	A5	A6
13	GND	GND
14	/IPLWRD	SA1
15	CS0	CS1
16	CS2	CS3
17	A11	/IPL0
18	/IPL1	/IPL2
19	IACK	/IPCYC
20	/CSIOD	/CSMEM
21	D0	D1
22	D2	D3
23	D4	D5
24	D6	D7
25	D8	D9
26	D10	D11
27	D12	D13
28	D14	D15
29	A3	A4
30	A1	A2
31	/ACKA	/ACKB
32	GND	GND

NOTES: This allows connection to a BVM IP Expansion Daughter Board (e.g. EXP100). The BVME4000/6000 architecture provides for a further 6 IP sites to be added via this extension interface. The interface allows full capability sites to be added including Interrupt Control, 32-bit operation 8MHz, 32MHz and CPU Synchronous speeds.

The interface is not intended for user connection, the pinout is provided here for reference only.

Appendix E Thermal Management

BVME4000	25 °C	50 °C	70 °C
25MHz MC68EC/LC040	No Heatsink No Airflow	No Heatsink No Airflow	No Heatsink 0.5m/s Airflow
33MHz MC68EC/LC040	No Heatsink No Airflow	No Heatsink Natural Airflow	No Heatsink 0.5m/s Airflow
25MHz MC68040	No Heatsink No Airflow	No Heatsink Natural Airflow	No Heatsink 0.5m/s Airflow
33MHz MC68040	No Heatsink Natural Airflow	No Heatsink 0.5m/s Airflow	Heatsink 1.0m/s Airflow

BVME6000	25 °C	50 °C	70 °C
50MHz MC68EC/LC060	No Heatsink No Airflow	No Heatsink No Airflow	No Heatsink 0.5m/s Airflow
66MHz MC68EC/LC060	No Heatsink No Airflow	No Heatsink 0.5m/s Airflow	No Heatsink 1.0m/s Airflow
50MHz MC68060	No Heatsink No Airflow	No Heatsink Natural Airflow	No Heatsink 0.5m/s Airflow
66MHz MC68060	No Heatsink Natural Airflow	No Heatsink 0.5m/s Airflow	No Heatsink 1.0m/s Airflow

NOTES: Temperatures shown above are for ambient air temperature.

If operation above 50 °C for extended periods is anticipated, then it is recommended that the airflow is doubled, or (where not already specified) a heatsink is fitted.

Where a heatsink is specified, fit AAVID part 3325 24 B 0 0032.

Appendix F Circuit Diagrams

NOTE: Circuit diagrams are provided here for customer *reference only*. This information was current at the time this User Manual was last revised. This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.

This is the master sheet for the
BVME4000/6000 rev F.

Processor and Memory
pro_mem.sch

2

This sheet contains:
- Processor socket
- SRAM
- EPROM
- MM Interface

Industry Pack Interface
ip.sch

5

This sheet contains:
- Industry Pack Interface
- IP Connectors
- EXP100 Connector

- Takes CPUCLK1

Power and Reset
pwr.sch

8

This sheet contains:
- 3.3 V Power Supply
- Reset Circuit
- Oscillator Circuit
- Battery Circuit
- General De-Couplers

Ethernet
eth.sch

3

This sheet contains:
- Ethernet Interface

- Takes CPUCLK1

VME Interface
vme.sch

6

This sheet contains:
- VME Interface
- P1 & P2 Connectors

SCSI
scsi.sch

4

This sheet contains:
- SCSI Interface

- Takes CPUCLK1

Peripherals and Interrupts
periph.sch

7

This sheet contains:
- Serial Port
- Parallel Port
- Real Time Clock
- Peripheral Control PAL
- Interrupt Control PAL

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Sheet 1 of 8

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Drawn By: **S J Bush**

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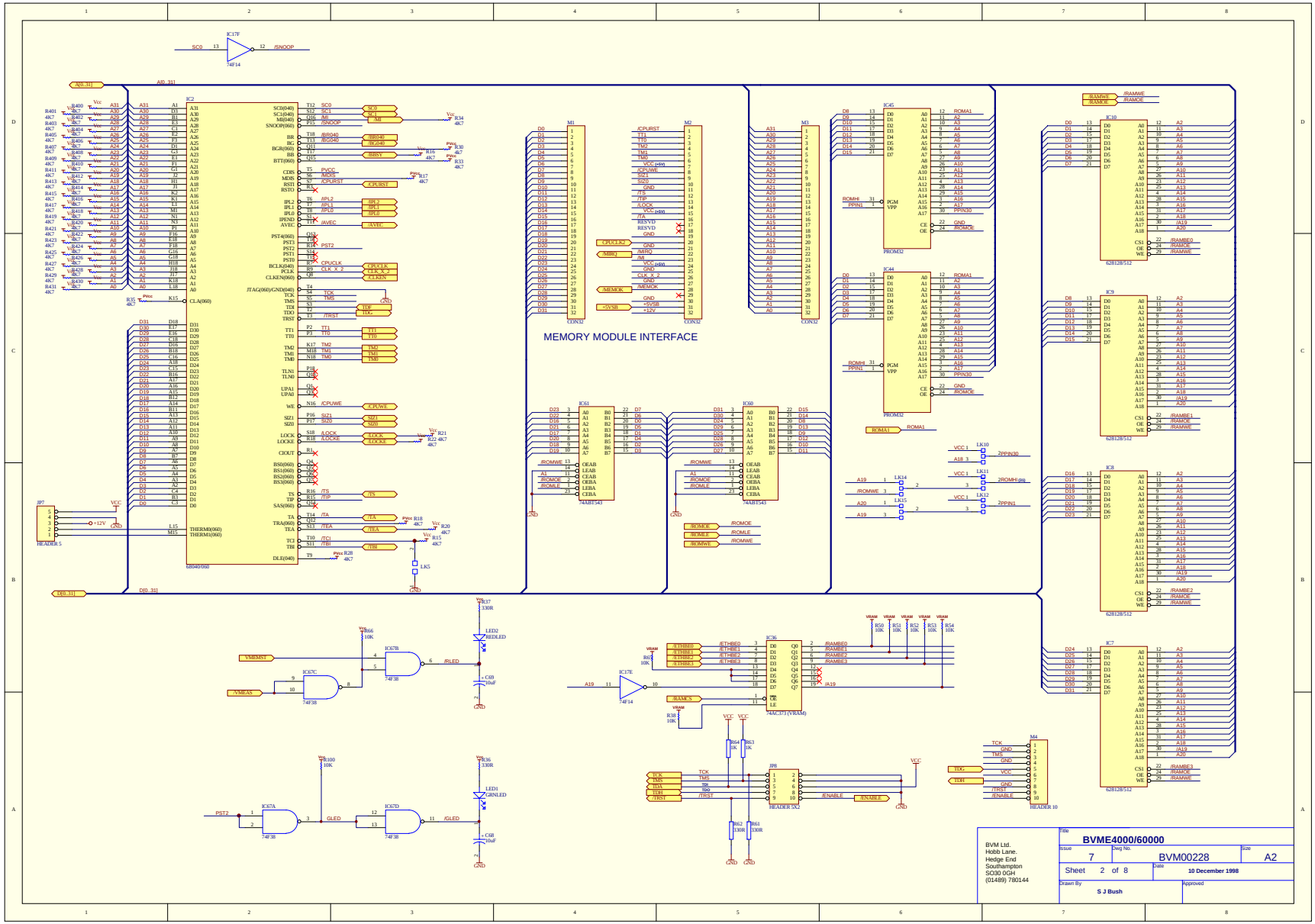
MEMORY MODULE INTERFACE
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Title
BVME4000/60000
Issue
7
Drwg No.
BVM00228
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A2
Sheet 2 of 8
Date
10 December 1998
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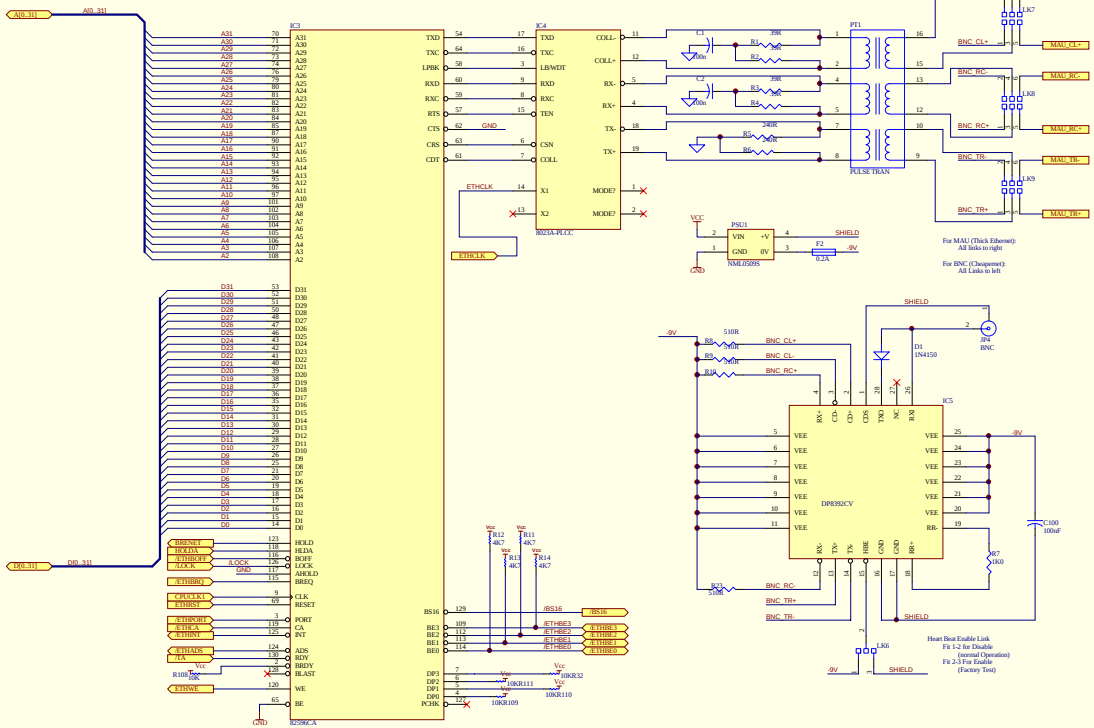
Approved



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	Sheet 3 of 8	Date: **10 December 1998**	
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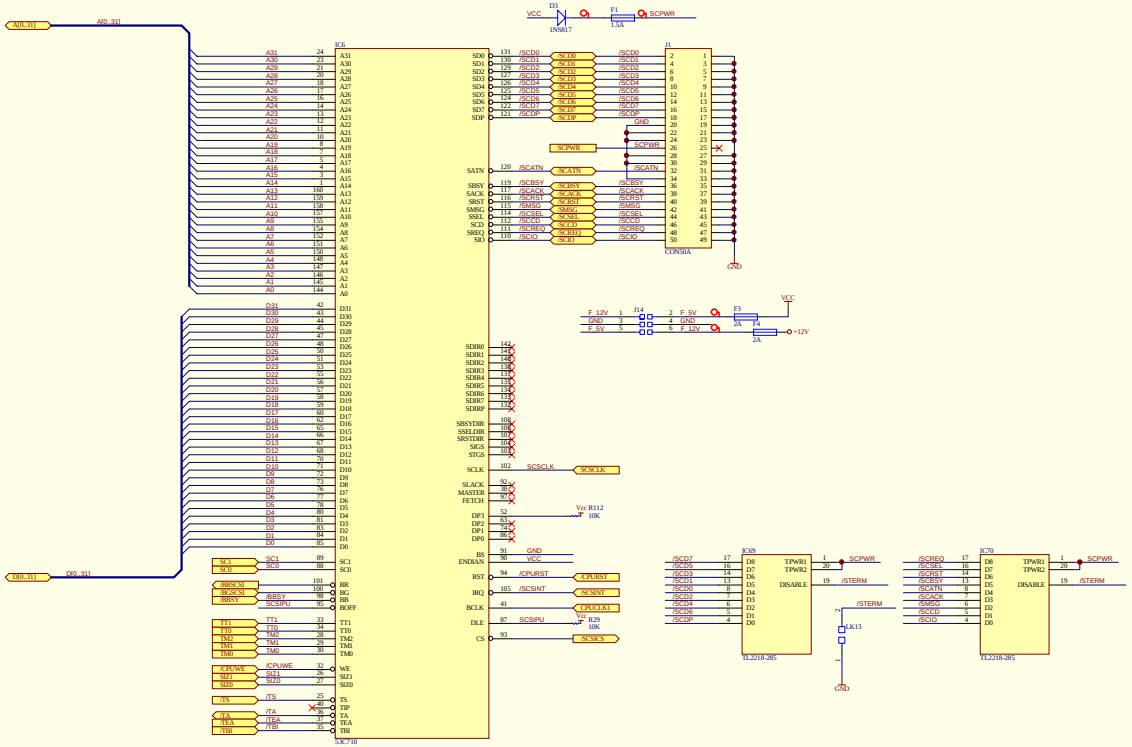

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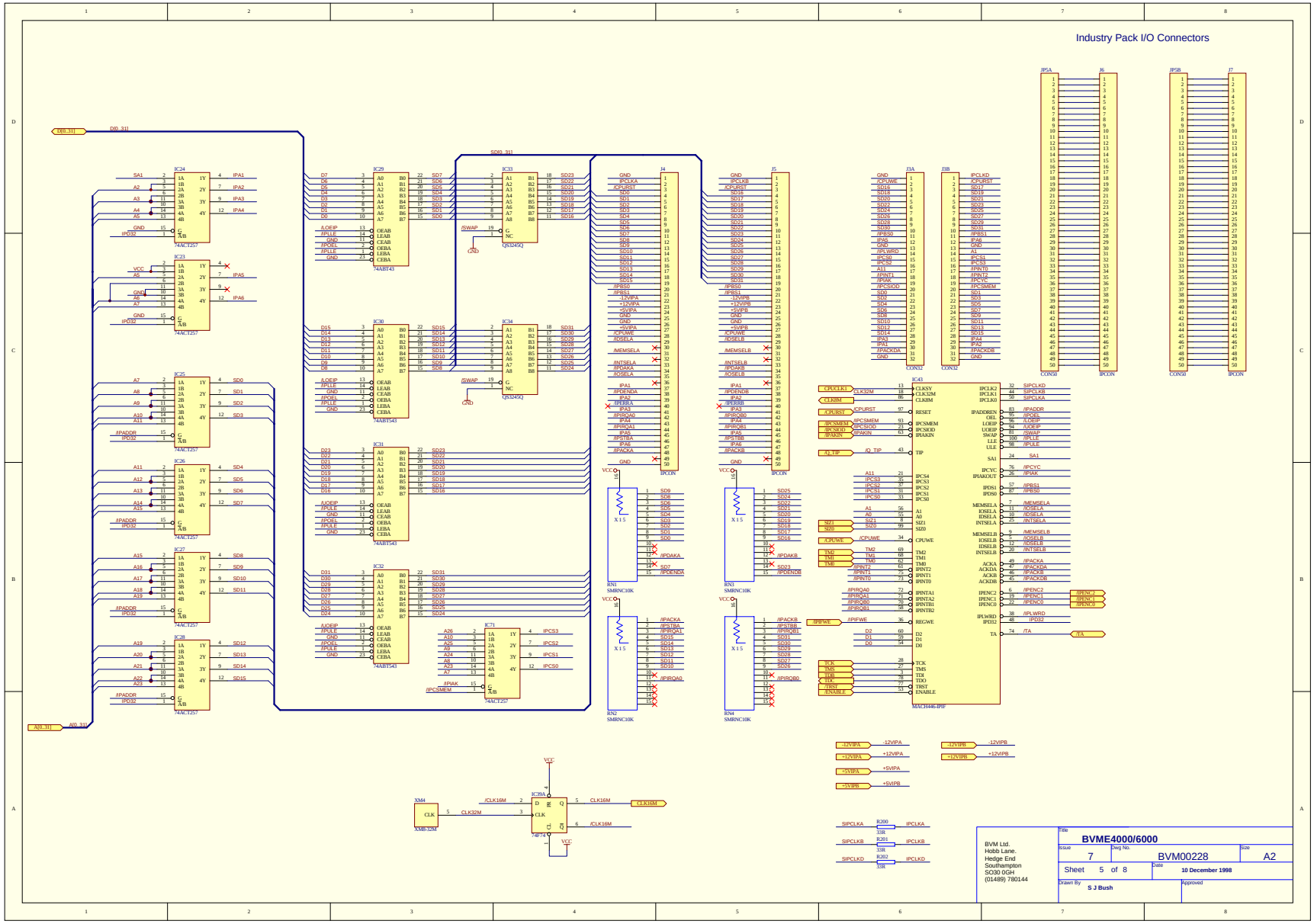
Industry Pack I/O Connectors
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Dwg No. BVM00228
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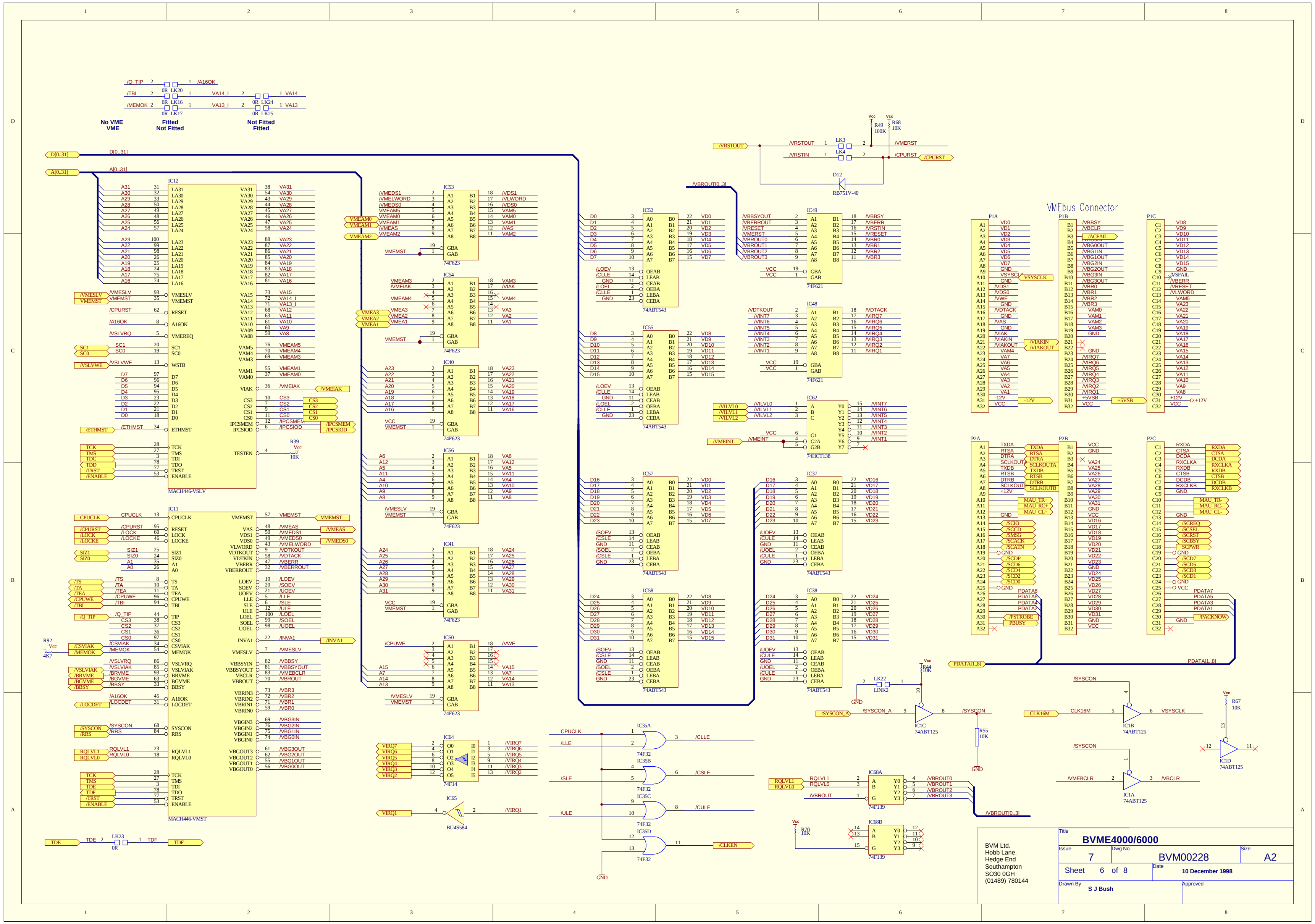
VMEbus Connector
No VME
VME
Fitted
Not Fitted
Not Fitted
Fitted
MACH446-VSLV
MACH446-VMST
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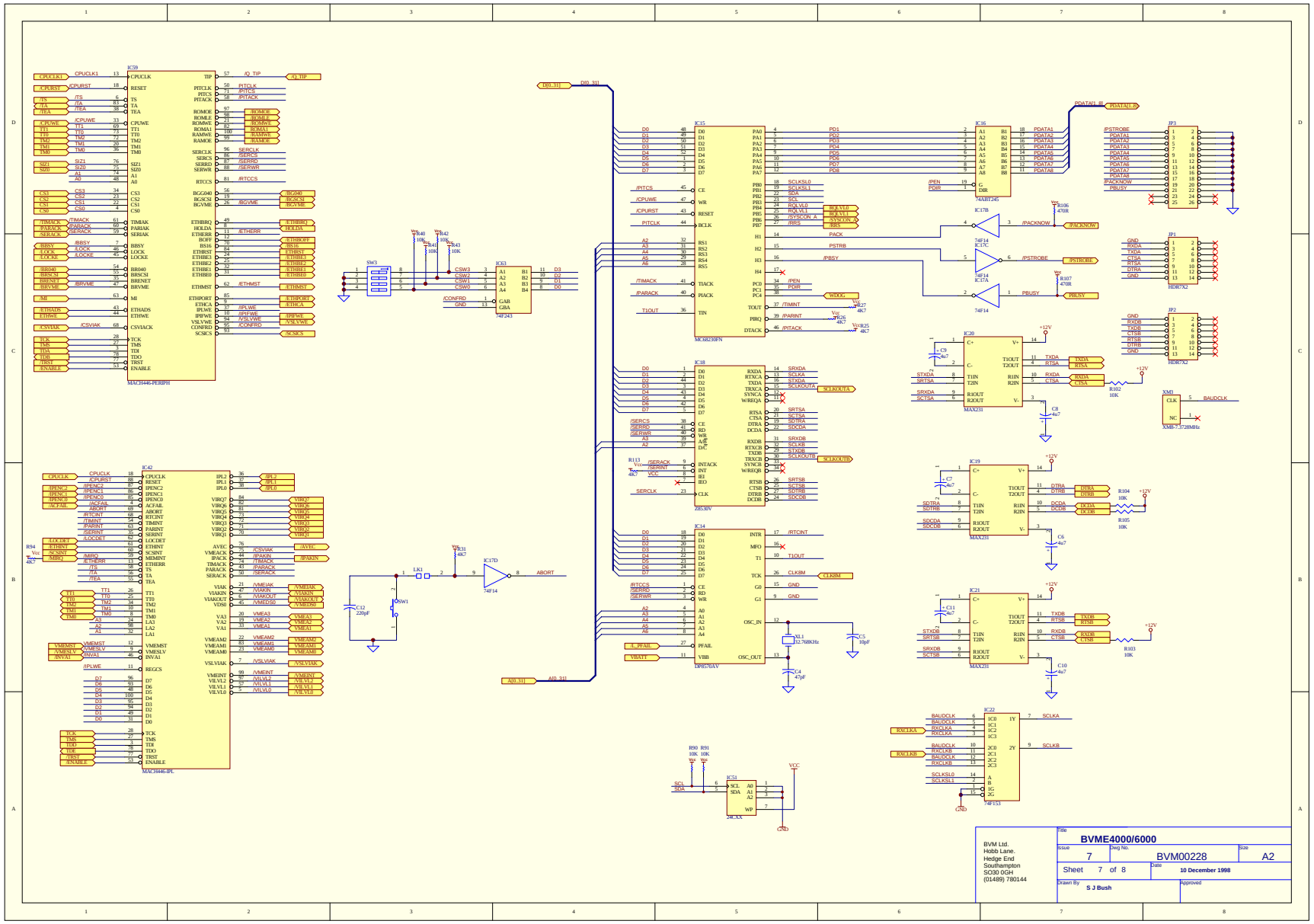
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IC42
MACH446-BPL
IC15
MC68230FN
IC18
IC14
28L30V
IC16
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IC17B
IC17C
74F14
IC17D
IC20
IC19
IC21
MAX231
IC22
74F153
IC63
74F243
IC51
24CXX
SW3
SW1
JP1
JP2
JP3
HDR7X2
HDR7X2
XMB
XMB-7.7728MHz
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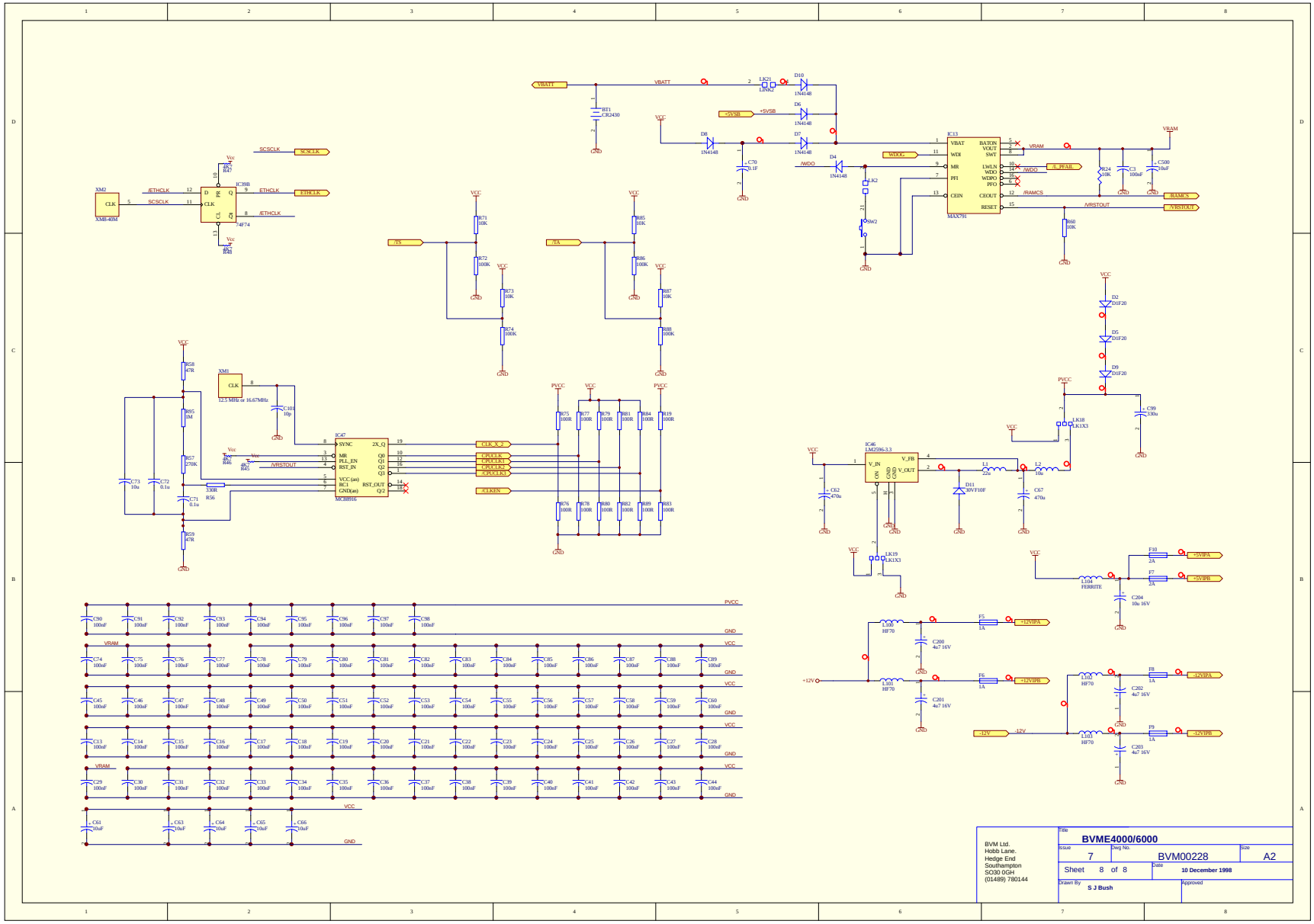

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