Manual P/N 454-48450

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User's Manual

BVME4500

MC68040 SINGLE BOARD
COMPUTER

Board Revision **B2**
Manual Revision **B 30 March 1998**

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R.F. INTERFERENCE

This product, in common with most other electronic equipment, generates, uses, and can radiate radio frequency energy. Operation of this equipment may cause radio interference, for which BVM Ltd can accept no responsibility.

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This product contains components which are susceptible to static discharge, and should be handled with appropriate caution.

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Include a return address and the telephone number of a technical contact, and a detailed description of the observed fault. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. BVM Ltd will not be responsible for damage due to improper packaging of returned items. Out of warranty repairs can be arranged, and will be charged on a material and labour basis, subject to a minimum repair charge. Return transportation and insurance will be charged as part of the repair and is in addition to the minimum charge.

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F) Although BVM Ltd offer a high level of technical support and advice, due to the complex nature and wide application of product configurations it is the responsibility of the purchaser to be satisfied at the time of purchase that the products are suitable for the final application.

G) The term 'Software' used herein is defined as 'any program data or code in source or binary format recorded in or on any readable device or media'.

H) BVM Ltd will effect all reasonable effort to resolve accepted reproducible software errors reported within 12 months of purchase. Acceptance of an error shall solely be based on conformance to supporting specifications. Proper operation of earlier releases is not guaranteed.

WARNINGS

Do not lever out memory modules from the BVME4500. The board uses surface-mounted devices extensively, which can be fractured by excessive force. Memory modules are not a field-fit option. **Damage may result if users attempt to remove or fit memory modules incorrectly.**

The BVME4500 uses devices sensitive to static electricity. Ensure adequate static electricity precautions are observed when handling the BVME4500, and memory modules.

Table Of Contents

1. Introduction

1.1. Scope

This manual provides :-
A getting started guide.
Configuration details.
A user reference guide.
A memory map.
A map of all register locations.
A detailed description of all dedicated registers.
Details of implementation specific considerations for major devices.
General hardware description.

This manual does not provide:-
Detailed data on the operation of the major devices.
Details of VMEbus Specifications.

Information is provided to allow the module to be integrated into a system and configured by the system software. This User Manual is intended for use by system integrators, service personnel, software engineers and end users.

Unless otherwise stated, address information is in hexadecimal notation.

1.2. BVME4500 Part Numbers

451-48450	MC68040 33MHz, 2Mb BOOTFLASH, 2Mb SRAM, VMEbus, ETHERNET.

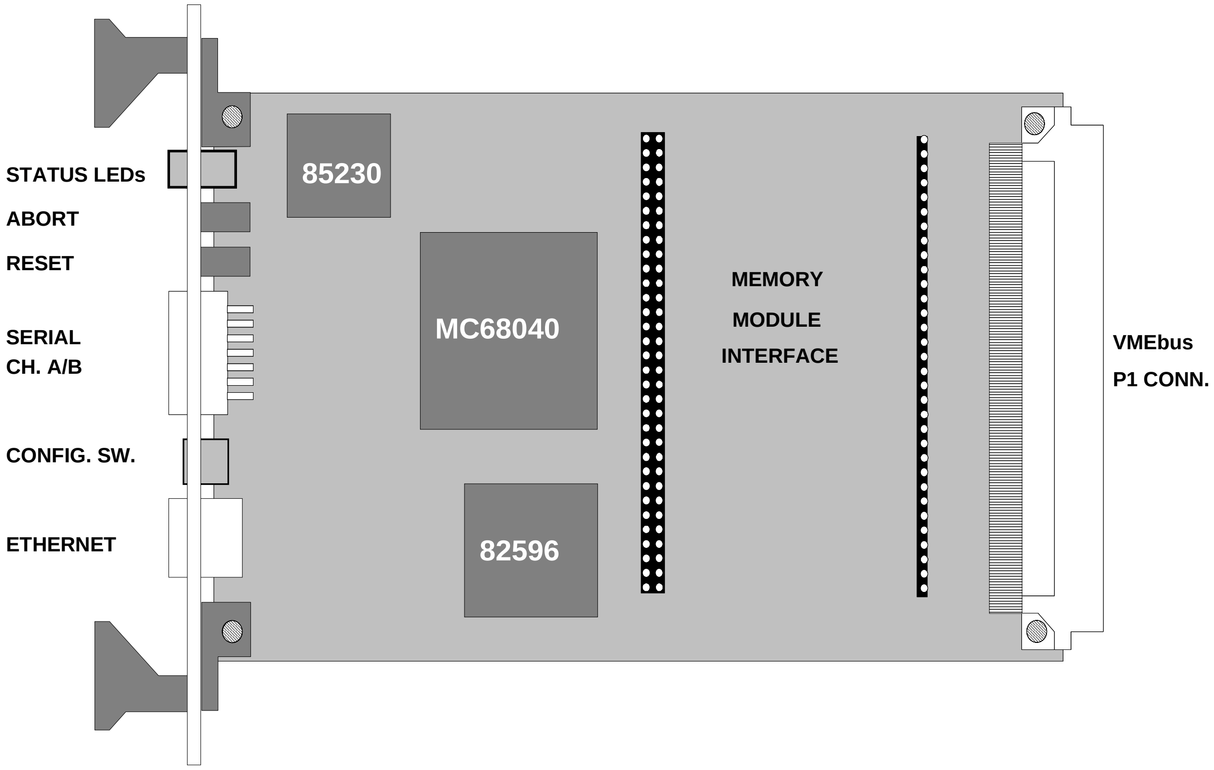
Other memory options are available, contact your supplier for details.

1.3. Memory Module (33MHz) Part Numbers

453-83391	MEM390 8Mbyte DRAM
453-83403	MEM400 16Mbyte DRAM & 4Mbyte FLASH
453-83404	MEM400 16Mbyte DRAM & 8Mbyte FLASH
453-83480	MEM480 16Mbyte DRAM
453-83481	MEM480 32Mbyte DRAM
453-83482	MEM480 48Mbyte DRAM

Other Memory Module options are available, contact your supplier for details.

2. Overview


STATUS LEDs
ABORT
RESET
SERIAL
CH. A/B
CONFIG. SW.
ETHERNET
85230
MC68040
82596
MEMORY
MODULE
INTERFACE
VMEbus
P1 CONN.

2.1. Features

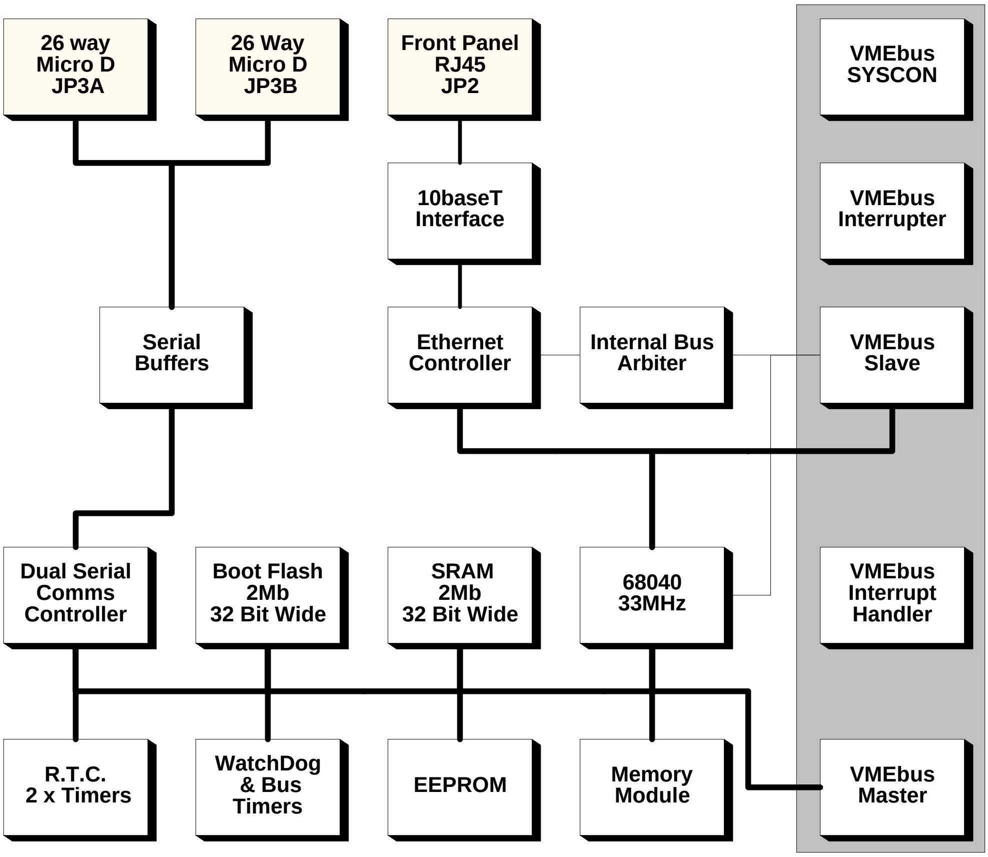
- MC68040 CPU.
  - 33MHz clock speed.
  - 4Kbyte data and instruction caches.
- 32-bit wide burst fill Dual Ported (with Bus Snooping) memory module interface with NO capacity limitations allowing many options, for example:
  - 8Mbytes of FLASH EPROM. Erasable, Programmable non volatile storage.
  - 48Mbytes DRAM.
- 2Mbyte 32-bit wide BOOTFLASH EPROM (2 x 16-bit wide AM29F800).
- 2Mbyte 32-bit non-volatile (battery backed) SRAM.
- 2Kbit EEPROM.
- High Performance DMA driven 10baseT Ethernet (82596CA).
- Two Interrupt driven serial I/O ports - RS232 (Z85230).
- Real Time Clock (Battery backed) Including Tick timer, 2 16-bit timers and non volatile configuration RAM (DP8570).
- Optimised A24,A16:D16,D08 master/slave VMEbus interface.
  - VMEbus Interrupter.
  - VMEbus Interrupt handler.
  - Location monitor - Mailbox Interrupts.
- VMEbus System Controller Functions.
  - Single level Arbiter (SGL).
  - RESET, SYSCLK generator.
- Status LED indicators.
- Single slot, 3U form factor.
- Full OS9 software support.
- Full VxWorks software support.
- Fully compatible to VMEbus specification revision C.1.
- Compatible with BVME4000/6000 series.

2.2. Applications

- VMEbus Main System Processor.
- VMEbus Intelligent I/O Processor.
- High Performance Embedded Processor.

3. Description

3.1. Block Diagram



3.2. Processor

The BVME4500 is based on the MC68040 32-bit processor from Motorola running at 33MHz. This virtual memory processor provides a MC68030 compatible integer processor running concurrently with an IEEE754 compatible floating-point unit (FPU). In addition two fully independent data and instruction demand page memory management units (MMUs) and two independent 4Kbyte caches provide efficient bus interface with a high degree of instruction execution parallelism.

3.3. Memory

The BVME4500 may be fitted with a large variety of 32-bit wide, burst fill memory devices. The BVME4500 uses the BVM memory module interface which provides a full 32-bit MC68040 bus, and supports 2/1/1/1 (no wait state) accesses to a variety of standard BVM memory modules, allowing use of memory modules which currently include:

- 8 to 48Mbytes DRAM (5/3/3/3 access at 33MHz bus clock).
- 16Mbytes DRAM plus 8Mbyte Flash EEPROM.

This memory can be dual ported (up to 16Mbytes) allowing concurrent accesses by both the processor and other VMEbus masters. These accesses may be 'snooped' by the processor to maintain cache coherency. This, together with the onboard 'location monitor' allows full multiprocessor communication with other CPU (and DMA) VMEbus cards.

The BVME4500 also provides 2Mbytes of 32-bit wide Static RAM (which can be battery-backed), requiring a six CPU clock cycle access. This SRAM may be used for non-volatile storage applications, or as main system memory in applications where a memory module is not fitted. The SRAM can also be dual ported to the VMEbus.

The BVME4500 has 2Mbytes of BOOTFLASH memory. The BOOTFLASH supports byte, word and longword accesses for read cycles, but only word and longword accesses for writes. All BOOTFLASH accesses require a six CPU clock cycle access.

The BVME4500’s internal address control registers can be accessed from the VMEbus whilst the CPU is held in a RESET condition when selected by switch. This allows the BOOTFLASH memory to be programmed from the VMEbus.

There is also an EEPROM with 2Kbits of storage available, which is accessed serially from special purpose registers in the BVME4500. This is typically used to store configuration data.

3.4. Real Time Clock

The BVME4500 provides a battery backed Real Time Clock using the DP8570 device. This device is battery backed, and maintains date and time data. The DP8570 can also generate an interrupt from it's periodic timer from 1mS to 1 second, or from two other independent 16-bit timers on chip. The timers offer a resolution of up to 500nS, and can be used in one-shot or periodic interrupt mode. A small amount of non-volatile storage is also provided for system configuration purposes. The DP8570 is battery backed using a lithium battery giving typically 10 years of non volatile operation (when SRAM backup is disabled).

3.5. Serial Communications

Two full-duplex independently buffered RS232 serial communications interfaces are provided from a Z85230 SCC device, supporting asynchronous baud rates of up to 115.2Kbit/s (using the on-board crystal) concurrently. The Z85230 has an 8 byte input buffer and a 4 byte output buffer, and the RTS, CTS, DTR and DCD RS232 control signals are also supported.

3.6. Ethernet Interface

An Ethernet Interface is provided built around the Intel 82596CA. This provides a 32-bit DMA driven interface to 10baseT Ethernet (via a front panel RJ-45). The 32-bit DMA driven interface allows direct access to the entire memory map of the BVME4500 allowing full packet management by the 82596CA. Each 32-bit transfer requires 320nS maximum (including arbitration) to execute the cycle. A transfer will occur no more frequently than every 4µS (4 bytes at 1Mbyte per second).

3.7. VMEbus Interface

Full VMEbus system controller functions are provided including SYSCLK drive, Bus time out monitor, SYSRESET drive and an efficient bus arbiter working in single level (SGL) arbitration mode.

3.7.1. VMEbus Master

Byte or Word Master accesses may be made to the Standard (A24) and Short I/O (A16) address spaces. BVME4500 Longword accesses to the A24 or A16 address space are converted to two Word cycles. Read Modify Write (RMW) cycles are supported for all of these accesses.

VMEbus arbitration is normally configured to be Release On Request (ROR) method. This may be changed to Release When Done (RWD) with a PLD change. Both schemes use FAIR requesting, ensuring each master has an equal chance of obtaining the bus. Digital bus busy filtering is used to ensure premium arbitration performance.

3.7.2. VMEbus Slave

The memory module and on-board SRAM are dual ported onto the VMEbus. The VMEbus base address, size of window and local base address are programmable for the A24 address space. The BVME4500 responds to Byte and Word Slave accesses to the A24 and A16 address spaces.

The BVME4500 can snoop VMEbus slave accesses if enabled to do so. Thus although the CPU uses extensive caching, full coherency is maintained by the CPU providing any data that is 'stale' in the accessed memory (see “Appendix B - CPU Cache Coherency and Bus Snooping”).

A VMEbus location monitor is also supported in the A16 address space. This is a fixed 256byte window size, and the VMEbus base address is programmable. A local interrupt can be enabled when the A16 VMEbus window is accessed.

The BVME4500 is compatible with VMEbus address pipelining and RMW cycles.

3.8. Interrupts

3.8.1. VMEbus Interrupt Handler

The BVME4500 may be configured to respond to VMEbus interrupts on any of the 7 VMEbus interrupt levels. Each interrupt level may be programmed to be enabled or disabled individually.

A User vectored VMEbus interrupt causes the CPU to reply with a VMEbus Master interrupt acknowledge cycle. The A1,2,3 address lines indicate the address level being handled.

The interrupting device returns an ID vector on the odd data byte. This is used as the user vector by the CPU.

3.8.2. Internal Interrupts

Internal CPU interrupts are generated from a variety of sources, as detailed in the table below:

Source	Level	Type
VMEIRQ7:1	IRQ7:1	Vectored
ACFAIL	7	Auto
ABORT	7	Auto
8570 RTC	6	Auto
MEMORY MODULE	4	Auto
85230 SCC	3	Vectored
82596CA ETHERNET	2	Auto
LOCATION MONITOR	1	Auto

3.8.3. VMEbus Interrupter

The BVME4500 may generate VMEbus interrupts on any programmable single level 1-7 and responds with a software programmable ID to the subsequent interrupt acknowledge cycle. Writing the ID to the a vector register causes a VMEbus interrupt to be generated on the selected level. The BVME4500 VMEbus interrupt ID vector may be programmed to suit the application.

3.9. VMEbus System Controller Functions

The BVME4500 provides a number of system controller functions that may be enabled by link selection.

RESET

Asserted if +5V falls below 4.7V and when a link is installed. VMEbus RESET has a minimum asserted period of 200mS.

ARBITRATION

The BVME4500 can be link selected to provide SGL VMEbus arbitration.

SYSCLK

The BVME4500 can be link selected to provide a 16MHz VMEbus SYSCLK.

BUS TIMER

The BVME4500 provides a 128µS Bus Timeout BERR signal when link selected to do so.

3.10. Power Supply Monitor/Watchdog

A MAX791 provides power up/power down control for the battery switching for the non volatile RAM and processor RESET. It also provides a processor watchdog capability such that, if enabled, the processor will be reset if the software fails to maintain pulses to the watchdog circuit.

3.11. Local Bus Monitor

All bus cycles (including VMEbus arbitration requests) are timed by an on-board timer. If any cycle takes longer than 64 CPU clock cycles, then a Transfer Error Acknowledge signal is generated and a bus error exception vector generated. Thus the processor cannot simply hang-up as a result of invalid addresses being generated from software. The exception to this is for VMEbus accesses; these are timed by the VMEbus Time out monitor.

3.12. Configuration Switch/Links

A 4-bit configuration selection is provided with a switch bit & 3 link selected bits for software bootstrap detection. This does not affect the hardware directly, but is normally used by the software to set up the BVME4500's configuration registers.

3.13. LED Indicators

Front panel indicators are provided for CPU running, Ethernet link active & VMEbus master accesses.

4. Installation

The BVME4500 module is inserted into a vacant VMEbus slot. If it is to function as the system controller, then it should be positioned in the left most slot. It passes through all VMEbus daisy chained arbitration signals.

IACK should be jumpered to IAKIN on the backplane in the left hand slot. All interrupt IAKIN to IAKOUT and BGIN to BGOUT signals should be jumpered across vacant slots to the left of the module.

If it is not the system controller, it may be located in any of the VMEbus slots to the right of the VMEbus system controller.

To install the BVME4500:

1. Ensure all backplane jumpers associated with the slot for the BVME4500 are removed.

2. Ensure the BVME4500 module is correctly configured for the target system.

3. Insert the BVME4500 module into the rack pushing the VMEbus connector fully home.

4. Secure the BVME4500 into the rack with the two fixing screws top and bottom.

5. Plug in serial cables to JP3.

6. If using Ethernet, connect the Ethernet RJ-45 connector to the BVME4500 RJ-45 connector.

7. Ensure that the configuration switch/links are set up correctly for the software installation.

Removal is the reverse of assembly.

If the test or application software fails, ensure that all installation instructions have been correctly carried out. Some typical reasons for incorrect operation are:-

1. The BVME4500 module uses the VMEbus Address modifier codes to determine address significance. Ensure the host CPU module produces the correct address modifier codes.

2. Ensure that all links are configured to the default set-up or that any alterations to the default are correctly configured.

3. Ensure that the VMEbus backplane (if used) is correctly configured with regard to the daisy-chain signal jumpers and the IACK termination jumpers (if any).

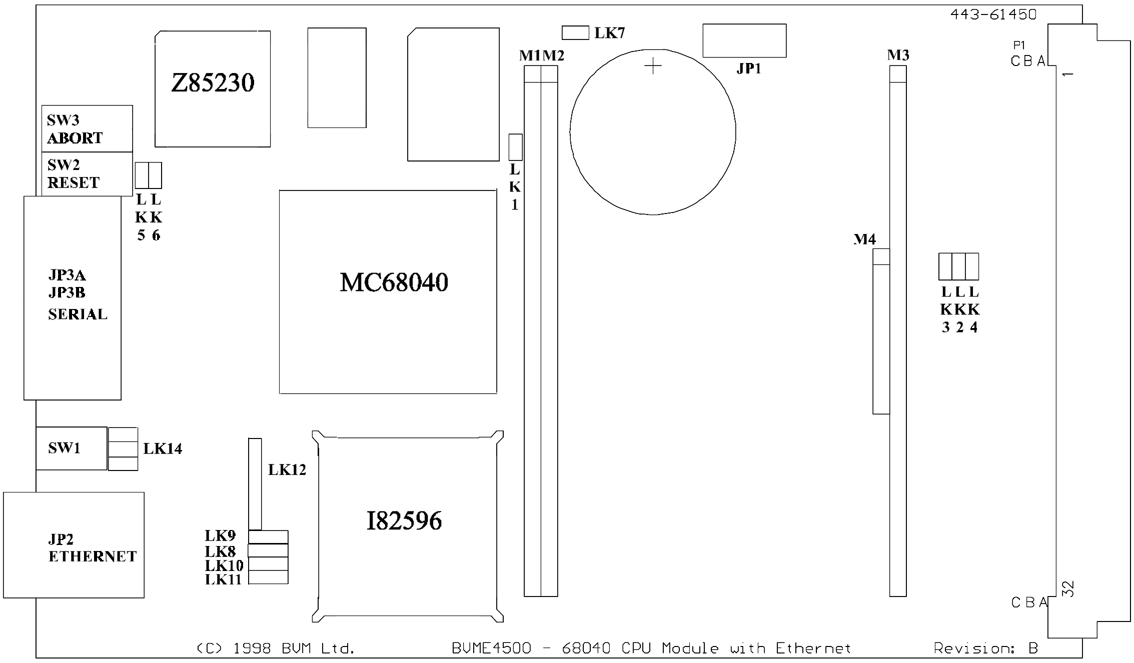
4. Check that the BOOTFLASH memory on the BVME4500 is correctly programmed with valid contents.

5. Check that SW1 POLE 2 (FPE) is OFF (away from PCB) which disables the slave access mode used to program the BOOTFLASH memory.

The BVME4500 CPU is fitted with a 9 °C/W heatsink (at 1.0m/s airflow). It is necessary to ensure adequate airflow across this heatsink to ensure correct operation of the BVME4500. See “8.7. Operating Environment” for further details.

5. Configuration

5.1. PCB Layout

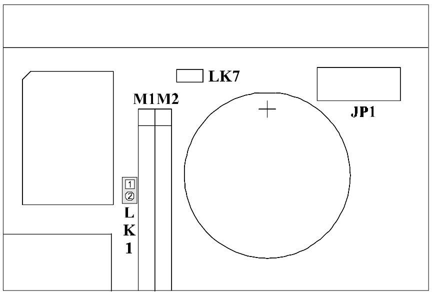


5.2. Link and Switch Definitions

The following link definitions show the links grouped in the same orientation as the layout drawing on the previous page, i.e. with the VMEbus connectors to the right. Link positions marked with a ✪ show the default configuration.

5.2.1. LK1 CPU Cache Inhibit

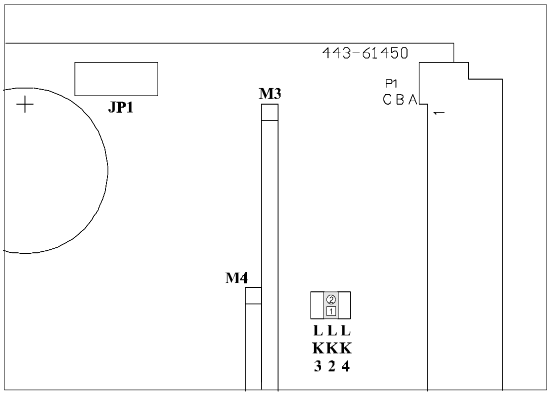
This link disables the MC68040's on chip data and instruction caches to allow (for example) emulators to be used with the BVME4500.



LK1	Function
1 & 2 Fitted	MC68040 CACHES DISABLED
1 & 2 Omitted ✪	MC68040 CACHES ENABLED

5.2.2. LK2 VMEbus Reset In Enable

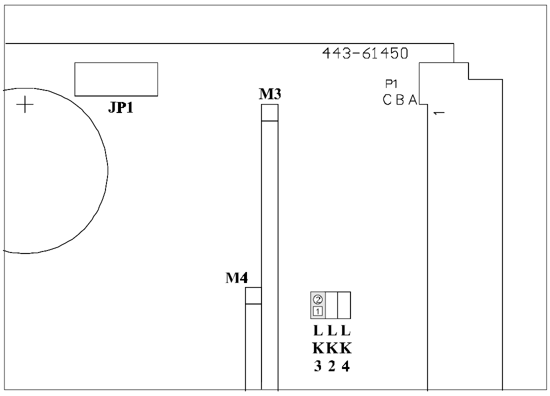
This link allows the BVME4500 to be reset from the VMEbus RESET signal.



LK2	Function
1 & 2 Fitted ✪	VMEbus RESET resets BVME4500
1 & 2 Omitted	NO BVME4500 RESET from VMEbus

5.2.3. LK3 VMEbus Reset Out Enable

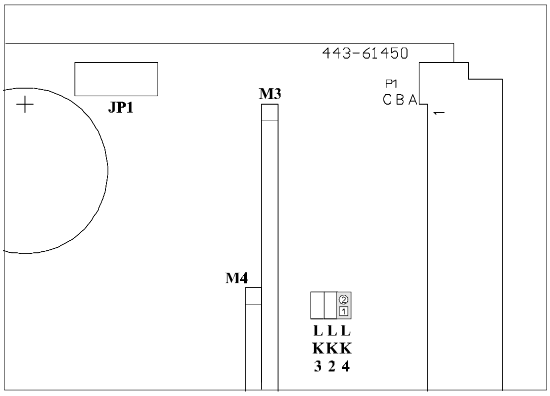
This link enables the VMEbus RESET to be driven by the BVME4500 RESET signal.



LK3	Function
1 & 2 Fitted ✪	BVME4500 RESET resets VMEbus
1 & 2 Omitted	NO VMEbus RESET from BVME4500

5.2.4. LK4 VMEbus System Controller Enable

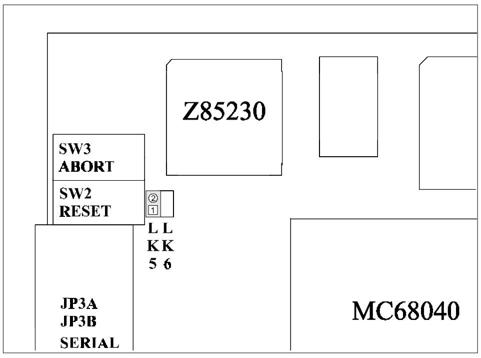
This link enables the BVME4500 as a VMEbus System Controller, driving the VMEbus SGL level arbiter, 16MHz VMEbus SYSCLK and 128µS Bus Timeout BERR signal.



LK4	Function
1 & 2 Fitted ✪	BVME4500 VMEbus System Controller ENABLED
1 & 2 Omitted	BVME4500 VMEbus System Controller DISABLED

5.2.5. LK5 Abort Switch Enable

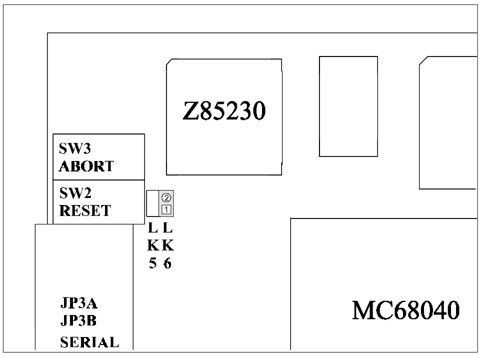
Fitting this link enables the ABORT switch to generate interrupts.



LK5	Function
1 & 2 Fitted ✪	ABORT Switch generates Level 7 Auto-vectored IRQ
1 & 2 Omitted	NO IRQ generated from switch

5.2.6. LK6 Reset Switch Enable

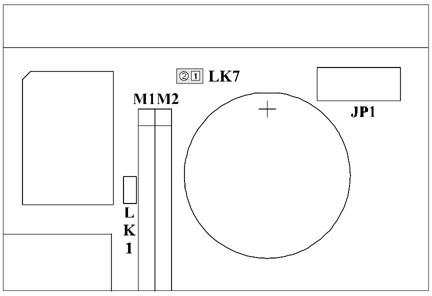
Fitting this link enables the RESET switch to generate a local reset and a VMEbus RESET if enabled (see “5.2.3. LK3 VMEbus Reset Out Enable”).



LK6	Function
1 & 2 Fitted ✪	RESET switch resets BVME4500 (and VMEbus)
1 & 2 Omitted	NO RESET generated from switch

5.2.7. LK7 SRAM Backup Selection

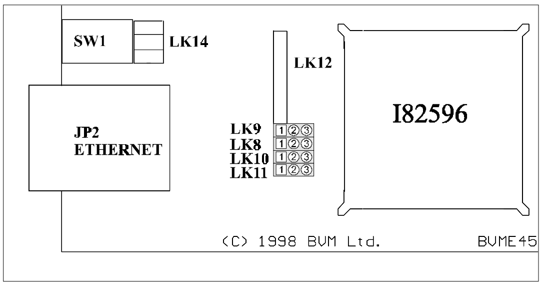
Fitting this link enables the SRAM to be backed up by the on-board battery. The SRAM is always backed up by the VMEbus STDBY supply.



LK7	Function
1 & 2 Fitted	SRAM is backed up by on-board battery or VMEbus STDBY
1 & 2 Omitted ✪	SRAM is only backed up by VMEbus STDBY

5.2.8. LK8,9,10,11 Ethernet Selection

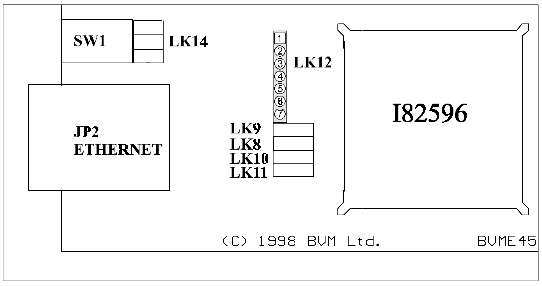
These links allow selection between 10baseT Ethernet (via front panel RJ-45 connector) or an optional Ethernet Expansion Interface on LK12. They must all be set in conjunction.



LK8,9,10,11	Function
1 & 2 ✪	10baseT Ethernet via front panel RJ-45
2 & 3	Ethernet via optional Ethernet Expansion Interface

5.2.9. LK12 Ethernet Expansion Interface

This is a header for an optional Ethernet expansion interface (NOT AUI).

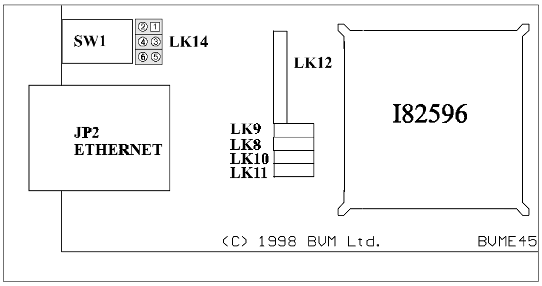


5.2.10. LK13 Factory Use Only

This is a **factory selectable link only**, not available to user's.

5.2.11. LK14 Configuration Links

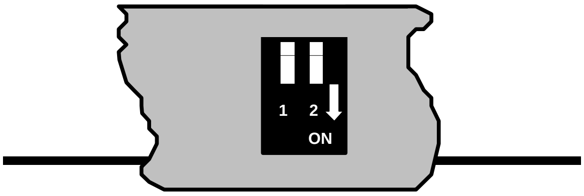
This link can be read by software to indicate system configuration options to the boot strap routines. A link FITTED selects a logical 0 for a bit and a link OMITTED selects a logical 1 for a bit. LK14 pins 1 & 2 relate to Bit 3, LK14 pins 3 & 4 to Bit 2, LK14 pins 5 & 6 to Bit 1 in the BVME4500 Configuration Switch Register (see "7.9.1. Configuration Switch Register").



5.2.12. SW1 Configuration Switch

CFG (POLE 1) of this switch can be read by software to indicate system configuration options to the boot strap routines. Switch ON (towards PCB) selects a logical 0 for bit 0 in the BVME4500 Configuration Switch Register and switch OFF selects a logical 1 for bit 0 (see "7.9.1. Configuration Switch Register")

FPE (POLE 2) of the switch is used to enable BOOTFLASH programming. When ON (towards PCB) the CPU is held in reset and the Address Control Registers on the board may be accessed from the VMEbus. The Address Control Registers can then be set up to allow VMEbus slave access to the BOOTFLASH memory on the BVME4500, which can then be programmed (see "7.8.6. Address Control Registers").



5.3. Indicators

5.3.1. Green LED - RUNNING

The GREEN RUNNING LED indicates that the BVME4500 is running valid code. When extinguished, the processor is either halted or stopped. The LED will also dim when the processor is executing an RTE instruction, stacking an exception frame or doing an MMU table search.

5.3.2. Yellow LED – Ethernet Link

The YELLOW ETHERNET LED indicates a valid Ethernet 10baseT connection.

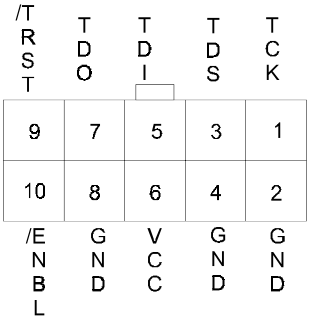
5.3.3. Red LED - VMEbus Master Access

The RED MASTER LED indicates that the BVME4500 is currently an active VMEbus master.

6. Connector Pinouts

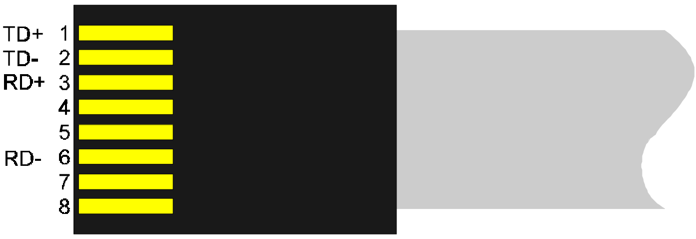
6.1. JP1 JTAG Connector

JP1 is a JTAG connection via a 2 x 5 way header, the pinout matching the Vantis MACH programming lead. This is for **factory use only**, to program the internal BVME4500 logic devices.



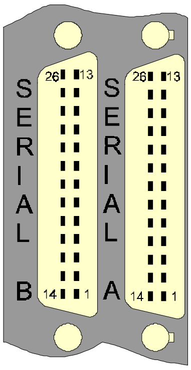
6.2. JP2 Ethernet Connector

JP2 provides a RJ-45 connection to a "twisted-pair" (IEEE802.3 10baseT) network. The pinout, shown to the right, is standard for connection to 10baseT directly.



6.3. JP3A & JP3B Serial Port Connections

Signal	JP3A/B Pin number	25-way D Pin number
GND	1	1
RxD	2	2
TxD	3	3
CTS	4	4
RTS	5	5
DTR	6	6
GND	7	7
DCD	8	8



JP3A and JP3B are 26-way sub-miniature D connectors which carry the serial port signals for Serial Channel A and Serial Channel B respectively. JP3B (Serial Channel B) is the connector nearest the PCB, JP3A (Serial Channel B) is the connector furthest from the PCB.

The pin-out is arranged to give a one to one connection to a 25-way D-type connector. Not all of the RS232 signals defined for a 25-way connector are supported by the BVME4500. The cable assembly should be built such that pins 1 to 8 on the 26 way connector connect to pin 1 to 8 of the 25-way D-type connector.

The JP3A/3B connector is an AMP 750821-1, with screw-lock posts AMP 750831-1 fitted on JP3B. A suitable mating connector is the AMP 750833-1 with back-shell AMP 750850-1 (6.35 – 7.11mm cable) or AMP750850-3 (7.11 – 7.87mm cable).

7. Programming

7.1. Address Map

The Address Map for the BVME4500 is shown below. The BVME4500 is byte addressed; each location addresses an 8-bit value. The BVME4500 supports full 32-bit addressing for all Local Bus Masters (the MC68040 CPU, the 82596CA LANC, and the VMEbus Slave Interface).

Some devices (BOOTFLASH, SRAM, VMEbus A24) are dual mapped. This is to allow the Transparent Translation registers in the MC68040 to provide alternative cache modes for accesses to these devices. The Cache Mode column is the suggested cache mode, the hardware provides no implicit cache mode control.

Address Range	Device	Size	Width	Cache Mode	Notes
00000000 - E7FFFFFF	Memory Module or SRAM	variable or (2Mb)	D32	copyback	1,3
E8000000 - E8FFFFFF	BOOTFLASH	16Mb (2Mb valid)	D32	write through	3,4
E9000000 - E9FFFFFF	SRAM (alternate)	16Mb (2Mb valid)	D32	write through	2,4
EA000000 - EDFFFFFF	Reserved	64Mb			
EE000000 - EEFFFFFF	VMEbus - A24:D16	16Mb	D16	write through	4
EF000000 - F7FFFFFF	Reserved	144Mb			
F8000000 - F8FFFFFF	BOOTFLASH	16Mb (2Mb valid)	D32	non-cached serial	3,4
F9000000 - F9FFFFFF	SRAM (alternate)	16Mb (2Mb valid)	D32	non-cached serial	2,4
FA000000 - FDFFFFFF	Reserved	64Mb			
FE000000 - FEFFFFFF	VMEbus - A24:D16	16Mb	D16	non-cached serial	4
FF000000 - FFFFFFFF	I/O see I/O map	16Mb		non-cached serial	

NOTES:

1 If 'RAMLO' is set, then accesses to the bottom 2Mb of this space access the Battery Backed SRAM.

2 If no memory module is fitted, this SRAM can be dual mapped, see note 1. The SRAM is always accessible at this location.

3 For the first two accesses after RESET, the EPROM is dual mapped at 00000000.

4 These spaces are dual mapped in order to allow different caching modes to be set up using the MC68040's Transparent Translation Registers.

7.1.1. I/O Address Map

Address Range	Device	Size	Width
FF000000 - FF0FFFFF	Reserved – bus error	1Mb	
FF100000 - FF1FFFFF	Ethernet Controller (LANC)	1Mb	D32
FF200000 - FF2FFFFF	Interrupt Control	1Mb	D8(OLW)
FF300000 - FF3FFFFF	Reserved – no bus error	1Mb	D8(OLW)
FF400000 - FF4FFFFF	VME Slave Access Control	1Mb	D8(OLW)
FF500000 - FF5FFFFF	Configuration Switch	1Mb	D8(OLW)
FF600000 - FF7FFFFF	Reserved – bus error	2Mb	
FF800000 - FF8FFFFF	Reserved – bus error	1Mb	
FF900000 - FF9FFFFF	RTC	1Mb	D8(OLW)
FFA00000 - FFAFFFFF	EEPROM / Watchdog Control	1Mb	D8(OLW)
FFB00000 - FFBFFFFF	SCC	1Mb	D8(OLW)
FFC00000 - FFDFFFFF	Reserved – bus error	2Mb	
FFE00000 - FFEFFFFF	Reserved – bus error	1Mb	
FFF00000 - FFFFFFFF	VMEbus A16	1Mb (64K wraps)	D16

7.2. Memory Module

Base Address	:	00000000.
Size	:	Memory Module Dependent.

The BVME4500 provides a site for BVM Memory Modules (refer to "Appendix C - Memory Module Pinout" for details). These modules are available in various configurations (DRAM, FLASH) and sizes and access speeds. Refer to the relevant Memory Module documentation detailed in the "Appendix A - Data Sheet & Manual References" section of this manual for details of the configuration.

The Memory Module Interface is 32-bits wide (though byte addressed) and supports Cache LINE transfers. Thus 'zero wait state' operation is supported; giving the MC68040 optimum performance of 2/1/1/1 clock cycles per transfer. Thus 16 bytes of data can be transferred in 5 clock cycles (100Mbyte/sec @ 33MHz bus clock). Refer to the relevant Memory Module Manual for actual memory performance.

The Memory Module provides a 'memory present' (/MEMOK) signal during the first cycle of an access that it decodes. Thus the BVME4500 address decoder automatically handles different size Memory Modules.

7.3. SRAM

Base Address	:	E9000000 or F9000000.
Size	:	2Mbyte.

The 2Mbytes of SRAM is 32-bits wide, and provides a 6 CPU clock cycle access. The SRAM can be accessed at the above two locations, which provide for different cache regions for the same memory. Normally the MC68040 will be set-up so that accesses in the region E9000000 - E9FFFFFF are write-through cached, and accesses in the region F9000000 - F9FFFFFF are non-cached with bus-serialised access. The SRAM is backed up by VMEbus STDBY and if selected, by the on-board battery. It is typically used for non-volatile storage applications such as a RAM-disc. The SRAM can retain it's data for up to 3 years from the battery.

The SRAM can also be mapped to appear at the bottom 2Mbytes of the memory map for boards without a memory module fitted by setting RAMLO. In this case the SRAM is used as main system memory, and normally will be treated as copy-back cached memory for maximum performance. Refer to “7.8. VMEbus Slave Access Controller” for RAMLO setting.

7.4. BOOTFLASH

Base Address	:	E8000000 or F8000000.
Size	:	2Mbyte.

The BVME4500 has 2Mbytes of BOOTFLASH memory using two AM29F800 TSOP devices. The BOOTFLASH supports byte, word and longword accesses for read cycles, but only word and longword accesses for writes.

All BOOTFLASH accesses require 6 CPU Clock cycles. The BOOTFLASH devices are internally divided into sectors. Two devices are required to produce a 32 bit-wide access, therefore the sector sizes are doubled. The address map to the right shows the sector sizes.

S18	128Kbytes
S17	128Kbytes
S16	128Kbytes
S15	128Kbytes
S14	128Kbytes
S13	128Kbytes
S12	128Kbytes
S11	128Kbytes
S10	128Kbytes
S9	128Kbytes
S8	128Kbytes
S7	128Kbytes
S6	128Kbytes
S5	128Kbytes
S4	128Kbytes
S3	64Kbytes
S2	16Kbytes
S1	16Kbytes
S0	32Kbytes

The BOOTFLASH can be accessed at the above two locations, which provide for different cache regions for the same memory. Normally the MC68040 will be set-up so that accesses in the region E8000000 - E8FFFFFF are write-through cached, and accesses in the region F8000000 - F8FFFFFF are non-cached with bus-serialised access.

The BOOTFLASH is also mapped at the bottom of the memory map for the first two cycles after a reset. This is to allow for the MC68040 to fetch the initial program counter and stack pointer from the first two longword locations in the BOOTFLASH.

For full programming details, refer to the AMD AM29F800 documentation detailed in the "Appendix A - Data Sheet & Manual References" section of this manual.

7.5. VMEbus Master Access

The BVME4500 can access VMEbus as a bus master. Depending on the Address Range used, different types of access are performed.

VMEbus specifies three basic Address Mode schemes - A16 (Short I/O), A24 (Standard) and A32 (Extended). The BVME4500 supports the A16 and A24 modes only.

VMEbus also specifies three basic Data Transfer schemes - D08(EO), D16 and D32. The BVME4500 supports the D08(EO) and D16 modes only.

The BVME4500 does not support Block transfers, A32:D32 or A64:D64.

7.5.1. A16:D16 (D08EO)

Base Address	:	FFFF0000.
Size	:	64Kbyte.

Accesses to this area perform a Short I/O access to VMEbus with LWORD inactive. Line and Long Word accesses are automatically broken down to Word (D16) cycles. Byte accesses produce a D08(EO) cycle.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Data Access	=	$2D
CPU User	Data Access	=	$29

7.5.2. A24:D16 (D08EO)

Base Address	:	FE000000 or EE000000.
Size	:	16Mbyte.

Accesses to this area perform a Standard Address access to VMEbus with LWORD inactive. Line and Long Word accesses are automatically broken down to Word (D16) cycles. Byte accesses produce a D08(EO) cycle.

The following Address Modifier (AM) codes are generated:

CPU Supervisor	Program Access	=	$3E
	Data Access	=	$3D
CPU User	Program Access	=	$3A
	Data Access	=	$39

7.6. Ethernet Controller

7.6.1. Overview

The Ethernet Interface is built around the Intel 82596CA LANC. This provides a 32-bit DMA driven interface to twisted-pair Ethernet (10baseT) via a front panel RJ-45 connector. The 32-bit, DMA driven interface allows direct access to the entire memory map of the BVME4500 allowing full packet management by the 82596CA. Each 32-bit transfer requires 320nS max (including arbitration) to execute the cycle. A transfer will occur no more frequently than every 4µS (4 bytes at 1Mbyte per second). Thus worst case bus bandwidth requirement is 11% at 33MHz bus clock.

7.6.2. Programming

The CPU and the 82596CA do not communicate directly (by registers). Instead, they communicate via a shared memory model. That is, the CPU sets up command blocks in memory and activates the 82596CA's Channel Attention. The 82596CA then examines the command block and executes the commands. When it has finished it generates an interrupt to the CPU.

The 82596CA is hardware configured for Big Endian operation. This has fairly subtle effects on parameter ordering in memory command blocks; in particular, most address pointers have their words swapped. For full programming details, refer to the 82596CA documentation detailed in the "Appendix A - Data Sheet & Manual References" section of this manual.

Although the CPU and the 82596CA do not generally communicate directly, there is a 'virtual' register that the CPU can access to assert Channel Attention and to write to an 82596CA internal register (PORT).

Refer to "Appendix B - CPU Cache Coherency and Bus Snooping" for details on Cache Coherency Implications (snooping) while the 82596CA is a bus master.

7.6.3. PORT Access

Accesses to the PORT register consist of **two consecutive 32-bit writes** at location **FF100000**, with bits D31..D16 of the command in the least significant word and bits D15..D0 of the command in the most significant word (i.e. the command is word-swapped). The PORT register is a write only register.

Writing to the 82596CA PORT allows the CPU to do four things:

1. Write an Alternative System Configuration Pointer (SCP) address. This needs to be done as the 82596CA will, by default, access 00FFFFF6 for its initial command block after reset.

2. Perform a dump of the internal state of the 82596CA to a specified address.

3. Execute a software reset.

4. Execute a self-test and write the results to memory at the specified address.

Function	D31		D4	D3	D2	D1	D0
Reset				0	0	0	0
Self-Test	A31	Self-test Results Area	A4	0	0	0	1
SCP	A31	Alternative SCP Address	A4	0	0	1	0
Dump	A31	Dump Area Pointer	A4	0	0	1	1

7.6.4. Channel Attention Access

Reading from location **FF100000** causes a pulse on the 82596CA Channel Attention input. This causes the 82596CA to execute command blocks.

7.6.5. Bus Error Handling

The 82596CA cannot directly handle bus errors. If the 82596CA is the bus master and accesses a location from which a bus error is generated (e.g. accesses non-existent memory) then special hardware on the BVME4500 handles the error condition.

When a bus error occurs, the 82596CA is removed from the bus and kept off the bus by asserting BOFF. ETHERR is generated causing an Ethernet Interrupt and the ETHERR bit to be set in the Interrupt Local Status Register (refer to "7.7. Interrupt Controller" for details of interrupt control and status). The 82596CA is held off the bus until a reset PORT command is issued to the 82596CA.

7.6.6. SYSBUS Byte Requirements

The SYSBUS byte of the SCP controls various hardware bus operations and must be set up as follows:

	Bit 6	Must be set.
INT	Bit 5	Must be clear (active high interrupt).
LOCK	Bit 4	LOCKed cycles are supported on the BVME4500. It is recommended that the LOCK function be enabled (bit is clear).
TRG	Bit 3	External Triggering is supported on the BVME4500. It is recommended that external triggering be used (bit is set).
M(1-0)	Bit 2,1	Should only be used in Linear Addressing Mode (bit 2 is set, bit 1 is clear).

7.6.7. Electrical Interface

The BVME4500 provides a full 'Twisted-Pair' (IEEE802.3 - 10BaseT) interface via the front panel RJ-45 connector. The BVME4500 also has an Ethernet Expansion Interface option, which can be used with additional circuitry to connect to a standard Ethernet AUI connection

Selection between the on board 10baseT interface or the Ethernet Expansion Interface is made by three links (refer to "5.2.8. LK8,9,10,11 Ethernet Selection" for details of the link settings).

7.7. Interrupt Controller

7.7.1. Overview

The Interrupt Controller is responsible for two independent functions:

Processor Interrupter	-	Takes interrupts from all sources (including VMEbus IRQs, Timers, Serial Ports etc.) and generates an interrupt to the CPU.
VMEbus Interrupter	-	Generates Interrupts on the VMEbus.

7.7.2. Processor Interrupter

Interrupt Source	Level	Type
ABORT Switch	7	Auto-vectored
8570 Timers	6	Auto-vectored
Memory Module	4	Auto-vectored
85230 DUART	3	Vectored
82596CA ENET	2	Auto-vectored
Location Monitor	1	Auto-vectored
VMEbus IRQ 7	7	Vectored. Individually maskable (see "7.7.4.1. VMEIRQ Enable Register").
VMEbus IRQ 6	6	
VMEbus IRQ 5	5	
VMEbus IRQ 4	4	
VMEbus IRQ 3	3	
VMEbus IRQ 2	2	
VMEbus IRQ 1	1	
VMEbus ACFAIL	7	Auto-vectored

Where multiple sources are generating interrupts on the same level, the acknowledge cycle is prioritised as follows:

Highest Priority:	Auto-vectored
	Local vectored
Lowest Priority:	VMEbus Interrupt

When a VMEbus Interrupt is acknowledged, the BVME4500 becomes a VMEbus master and initiates an Interrupt Acknowledge cycle over VMEbus. The BVME4500 expects the VMEbus interrupter to return a vector which is then used by the processor vectoring mechanism. If no VMEbus interrupter responds within the VMEbus time-out period, then a 'spurious interrupt' vector is generated.

7.7.3. VMEbus Interrupter

The BVME4500 can generate interrupts on the VMEbus. This function is completely independent of the processor Interrupter function. When acknowledged by the VMEbus interrupt handler, the BVME4500 returns a programmable 8-bit vector. The interrupter is implemented as Release On AcKnowledge (ROAK). Thus the interrupt is cleared by the interrupt acknowledge cycle.

The BVME4500 may generate an interrupt on any of the seven VMEbus IRQ levels. However, it can only generate on a single level at any one time. The level on which an interrupt is generated is programmable (refer to "7.7.4.3. VMEIRQ Level Register" below).

The interrupt is asserted by the processor writing to the VMEIRQ Vector Register (refer to "7.7.4.2. VMEIRQ Vector Register" below). The value written to the VMEIRQ Vector Register is then used as the value returned in the subsequent acknowledge cycle.

7.7.4. Interrupt Controller Registers

The Interrupt Controller contains six byte wide registers in four I/O locations. The first three locations are WRITE ONLY - DO NOT READ FROM THEM, the last location is READ ONLY.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF200003	VMEIRQ Enable	VIEN7	VIEN6	VIEN5	VIEN4	VIEN3	VIEN2	VIEN1	ACFEN
FF200007	VMEIRQ Vector	VEC7	VEC6	VEC5	VEC4	VEC3	VEC2	VEC1	0
	VMEIRQ Level	Rsrvd	Rsrvd	Rsrvd	Rsrvd	VLVL2	VLVL1	VLVL0	1
FF20000B	LOCIRQ Enable	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	LOCEN	0
	ETHIRQ Enable	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	ETHEN	1
FF20000F	Local IRQ Status	Rsrvd	Rsrvd	Rsrvd	Rsrvd	ABORT	ACFAIL	ETHERR	ETHIRQ

7.7.4.1. VMEIRQ Enable Register

Bit 7-1: **VIEN(7-1): VMEbus Interrupt Enable.**
When SET, these bits enable the corresponding interrupts from VMEbus. For example setting bits 7 and 3 enable VMEbus IRQs 7 and 3 to generate interrupts to the processor.

After RESET, these bits are CLEAR (i.e. all VMEbus interrupts disabled).

Bit 0: **ACFEN: ACFAIL Interrupt Enable.**
When SET, this bit enables interrupts from the VMEbus ACFAIL signal. See “7.7.4.6. Local IRQ Status Register” for details on ACFAIL interrupt operation.

After RESET, this bit is CLEAR (i.e. ACFAIL interrupts disabled).

7.7.4.2. VMEIRQ Vector Register

Bit 7-1: **VEC(7-1): Interrrupt Vector.**
Writing to this register sets bits 7 to 1 of the Interrupt ID vector that will be returned to the VMEbus Interrupt Handler, bit 0 is always set to ZERO. The act of writing to this register also causes the VMEbus interrupt line, selected by the LVL(2-0) bits in the VMEIRQ Level Register, to become active.

Bit 0: **Select Bit.**
This bit is used to select between the VMEIRQ Level Register and the VMEIRQ Vector Register. This bit must be written as a **ZERO** to select the VMEIRQ Vector Register.

7.7.4.3. VMEIRQ Level Register

Bit 7-4: **Reserved.**
For future compatibility these must be always written as zero.

Bit 3-1: **VLVL(2-0): VMEbus Interrupter Level.**
These bits select on which VMEbus Interrupt level the board will act as an interrupter. The binary code written selects the corresponding interrupt level (i.e. 101 selects level 5). When set to 000, no interrupt can be generated on VMEbus.

After RESET, these bits are CLEAR (i.e. VMEbus interrupt generation disabled).

Bit 0: **Select Bit.**
This bit is used to select between the VMEIRQ Level Register and the VMEIRQ Vector Register. This bit must be written as **ONE** to select the VMEIRQ Level Register.

7.7.4.4. LOCIRQ Enable Register

Bit 7-2: **Reserved.**
For future compatibility these must be always written as zero.

Bit 1: **LOCEN: Location Monitor Interrupt Enable.**
When SET, this bit enables interrupts from the VMEbus Location Monitor (refer to "7.8. VMEbus Slave Access Controller" for details of VMEbus Slave Operation).

After RESET, this bit is CLEAR (i.e. location monitor interrupts disabled).

This bit is used to clear the Location Monitor Interrupt during interrupt service routines. The interrupt is cleared by disabling (CLEARing) and re-enabling (SETting) the Location Monitor Interrupt.

Bit 0: **Select Bit.**
This bit is used to select between the LOCIRQ Enable Register and the ETHIRQ Enable Register. This bit must be written as **ZERO** to select the LOCIRQ Enable Register.

7.7.4.5. ETHIRQ Enable Register

Bit 7-2: **Reserved.**
For future compatibility these must be always written as zero.

Bit 1: **ETHEN: Ethernet Interrupt Enable.**
When SET, this bit enables interrupts from the 85296 Ethernet Controller (Refer to "7.6. Ethernet Controller" for details of Ethernet Controller Operation).

After RESET, this bit is CLEAR (i.e. 82596CA interrupts disabled).

This bit is used to clear the 82596CA Interrupt during interrupt service routines. The interrupt is cleared by disabling (CLEARing) and re-enabling (SETting) the Ethernet Interrupt.

Bit 0: **Select Bit.**
This bit is used to select between the LOCIRQ Enable Register and the ETHIRQ Enable Register. This bit must be written as a **ONE** to select the ETHIRQ Enable Register.

7.7.4.6. Local IRQ Status Register

Bit 7-4: **Reserved.**
These bits are unused. When read, their state is undefined.

Bit 3: **ABORT: Abort Switch Interrupt.**
This bit indicates the status of the ABORT switch. If this bit is SET, the ABORT switch is pressed. This will also generate an Auto-vector level 7 interrupt, so this bit can be used to determine that the ABORT switch was the source of an Auto-vector level 7 interrupt.

Bit 2: **ACFAIL: VMEbus ACFAIL Interrupt.**
This bit indicates the status of the VMEbus ACFAIL signal. If this bit is SET, the ACFAIL signal is active. This will also generate an Auto-vector level 7 interrupt, so this bit can be used to determine that the ACFAIL signal was the source of an Auto-vector level 7 interrupt.

Bit 1: **ETHERR: Ethernet ERROR Interrupt.**
This bit indicates that a 82596CA Ethernet Controller BUS ERROR has occurred. Refer to "7.6.5. Bus Error Handling" for further details.

Bit 0: **ETHIRQ: Ethernet Interrupt Level.**
This bit indicates the status of the 82596CA Ethernet Controller interrupt signal. If this bit is SET, the 82596CA's interrupt signal is active. **Note:** This does not indicate the status of the internal interrupt signal controlled by ETHEN, but indicates the status of the 82596CA's interrupt signal directly. The 82596CA will pulse its interrupt line inactive whenever a 'new' interrupt condition becomes true within the device. Thus to distinguish between an Ethernet Error interrupt and a normal Ethernet interrupt, the ETHERR bit should be interrogated; not the ETHIRQ bit.

7.8. VMEbus Slave Access Controller

7.8.1. Overview

The BVME4500 allows other VMEbus masters to access some of its onboard address space. It allows accesses via A24 address spaces. The BVME4500 also acts as a location monitor for A16 accesses.

7.8.2. Standard (A24) Accesses

Both the size of the window and the base address of the window (from the VMEbus master's point of view) are programmable. The base address of the access from the onboard memory's point of view is also programmable.

Thus the BVME4500 can be set-up to 'dual map' a programmable amount of memory (64Kbyte to 16Mbyte) onto the VMEbus. The local base address of the memory is programmable (on window size boundaries). The address that the 'dual mapped' memory appears at on VMEbus is also independently programmable. So, for example, 512Kbytes of memory module memory located at 00380000 could be accessed by another VMEbus master accessing location 00C00000-00C80000.

The A24 address works by comparing the most significant byte of the address with the programmed base address, thus A24 space is programmable on 64Kbyte (2^{16}) boundaries.

The window sizing operates by masking out address bits to the comparator. Thus for A24 space the smallest window size (when no bits are masked) is 64Kbyte. The window sizes available are powers of two up to the maximum window size of the address space (A24 = 16Mbytes).

A restriction on the window base address is that it must be on a window size boundary. Thus if the window size is 128Kbytes, the window base address must be on a 128Kbyte boundary, e.g. 00000000, 00020000, 00040000, 00D00000 etc.

The BVME4500 responds to the following A24 Address Modifiers (AM) codes:

CPU Supervisor	Program Access	=	$3E
	Data Access	=	$3D
CPU User	Program Access	=	$3A
	Data Access	=	$39

7.8.3. Short I/O (A16) Accesses

The BVME4500 will respond to Short I/O (A16) accesses. The size of the window is fixed at 256bytes. The base address is programmable on 256byte boundaries.

Short I/O space accesses act as a location monitor only and do not access physical memory within the BVME4500. This space is used to allow 'mail box' interrupts to the processor on the BVME4500. This allows other bus masters to use semaphore control with the BVME4500 without the use of the VMEbus IRQ lines.

The BVME4500 responds to the following A16 Address Modifiers (AM) codes:

CPU Supervisor	Data Access	=	$2D
CPU User	Data Access	=	$29

7.8.4. Controlling The Window Size

The table below shows window sizes for valid combinations of the Mask Register:

Mask Register	A24 Address Space Window Size
00	64Kb
01	128kb
03	256kb
07	512Kb
0F	1024Kb
1F	2048Kb
3F	4096Kb
7F	8192Kb
FF	16384Kb

7.8.5. Local Address Generation

The Local Base Address register (A24LBA) contains the base address of the 'dual mapped' memory window.

For A24 accesses, the most significant eight local address lines are driven by the **A32LBA** register. The unmasked (see A24MSK register description) A24 Local Base Address (A24LBA) Register bits are used as the next most significant address lines during the VMEbus slave access to the onboard memory. All other local address lines are driven from the VMEbus Address bus.

Thus for standard (A24) VMEbus accesses both the A32LBA and the A24LBA registers need to be set up.

7.8.6. Address Control Registers

Slave accesses are controlled by six byte wide **write only** registers.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF420003	A24VBA	A23cmp	A22cmp	A21cmp	A20cmp	A19cmp	A18cmp	A17cmp	A16cmp
FF430003	A24MSK	A23msk	A22msk	A21msk	A20msk	A19msk	A18msk	A17msk	A16msk
FF440003	A16VBA	A15cmp	A14cmp	A13cmp	A12cmp	A11cmp	A10cmp	A9cmp	A8cmp
FF450003	A32LBA	A31ladd	A30ladd	A29ladd	A28ladd	A27ladd	A26ladd	A25ladd	A24ladd
FF460003	A24LBA	A23ladd	A22ladd	A21ladd	A20ladd	A19ladd	A18ladd	A17ladd	A16ladd
FF470003	ADDRCTL	Reserved	Reserved	SCVME	SCETH	Reserved	A24EN	A16EN	RAMLO

7.8.6.1. A24VBA - A24 VMEbus Base Address Register

This contains an 8-bit value, against which standard (A24) VMEbus accesses are matched in order to determine slave access. If VMEbus A[23..16] matches, then an access to the onboard memory is performed.

7.8.6.2. A24MSK - A24 VMEbus Address Mask Register

This contains an 8-bit mask that is applied, on a bit by bit basis, to the VMEbus slave address decoding for A24 (standard) accesses from another VMEbus master. If a bit is set (a 1) then the corresponding address line is ignored. Thus the contents of this register control the size of the window decoded by the BVME4500 (refer to "7.8.4. Controlling The Window Size" for more details).

7.8.6.3. A16VBA - A16 VMEbus Base Address Register

This contains an 8-bit value, against which A16 VMEbus accesses are matched in order to determine slave access. If VMEbus A[15..8] matches, then a Short I/O access is performed.

7.8.6.4. A32LBA - A32 Local Base Address Register

This contains an 8-bit value that is used to drive the onboard most significant address lines during an access by another VMEbus master. In other words it contains the most significant part of the local memory base address of the 'dual mapped' window (refer to "7.8.5. Local Address Generation**"** for more details).

7.8.6.5. A24LBA - A24 Local Base Address Register

This contains an 8-bit value that is used to drive the onboard next most significant address lines during an access by another VMEbus master. In other words it contains the next most significant part of the local memory base address of the 'dual mapped' window (refer to "7.8.5. Local Address Generation" for more details).

7.8.6.6. ADDRCTL - Address Control Register

This contains some miscellaneous control bits, After RESET all bits are CLEAR.

Bit 7-6: **Reserved.**
For future compatibility this must be always written as zero.

Bit 5: **SCVME: VMEbus Snoop Control.**
This bit enables snooping for VMEbus Slave Accesses. When SET, VMEbus slave accesses are snooped by the CPU, so that the CPU will sink and source dirty data (refer to "Appendix B - CPU Cache Coherency and Bus Snooping" for a discussion on snooping and cache coherency).

Bit 4: **SCETH: Ethernet Snoop Control.**
This bit enables snooping for Ethernet Controller Master Accesses. When SET, Ethernet Controller master accesses are snooped by the CPU, so that the CPU will sink and source dirty data (refer to "Appendix B - CPU Cache Coherency and Bus Snooping" for a discussion on snooping and cache coherency).

Bit 3: **Reserved.**
For future compatibility this must be always written as zero.

Bit 2: **A24EN: VMEbus A24 Slave Access Enable.**
When SET VMEbus A24 slave accesses are enabled as specified by the A24VBA, A24MSK, A24LBA & A32LBA registers. When CLEAR VMEbus A24 slave accesses are disabled.

Bit 1: **A16EN: VMEbus A16 Slave Access Enable.**
When SET VMEbus A16 slave accesses are enabled as specified by the A16LBA register. When CLEAR VMEbus A16 slave accesses are disabled.

Bit 0: **RAMLO: Map RAM Low.**
When SET, the SRAM (located at E9000000 and F9000000) is also mapped at 00000000. This is mainly intended to provide a common address map for systems with no memory module fitted.

7.8.6.7. Register Access from VMEbus

When **FPE** (POLE 2) of SW1 is ON (towards PCB) the CPU is held in reset and the Address Control Registers on the board may be accessed from the VMEbus (see "5.2.12. SW1 Configuration Switch"). The Address Control Registers can then be set up to allow VMEbus slave access to the BVME4500.

The equivalent VMEbus addresses of the registers in A16 address space are shown below. The BVME4500 will appear as a block in A16 address space from F000 to F7FF, but should only be accessed at the **write only** locations shown below. The register functions are exactly as described above.

Local Address	VMEbus Address	Register
FF420003	F203	A24VBA
FF430003	F303	A24MSK
FF440003	F403	A16VBA
FF450003	F503	A32LBA
FF460003	F603	A24LBA
FF470003	F703	ADDRCTL

This function is primarily used for programming the on-board BOOTFLASH memory from the VMEbus. A typical setup for this would write C0 to A24VBA (VMEbus A24 address C00000), F8 to A32LBA (BOOTFLASH local address F8000000) and 04 to ADDRCTL (A24 enable), with the other registers in default condition. See "7.4. BOOTFLASH" for more BOOTFLASH programming details.

7.9. Configuration Switch & Links

This is a combination of POLE1 of SW1 (CFG) and three links on LK4 giving 4 configuration bits. The bits have no dedicated hardware function. They are provided to allow configuration selection within software applications. The state of each bit can be read in the Configuration Switch Register.

See "5.2.11. LK14 Configuration Links" and "5.2.12. SW1 Configuration Switch" for further information on setting these bits.

7.9.1. Configuration Switch Register

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FF500003	CONFSW	Reser-ved	Reser-ved	Reser-ved	Reser-ved	LK14 1 & 2	LK14 3 & 4	LK14 5 & 6	SW1 POLE1 (CFG)

Bit 7-4: **Reserved.**
These bits are unused. When read, their state is undefined.

Bit 3-0: **LK14/SW1.**
Reflects the state of the relevant switch or link. When the switch is ON (towards PCB) or the link is FITTED, the associated bit is read as ZERO. When the switch is OFF (away from PCB) or the link is OMITTED, the associated bit is read as ONE.

7.10. Real Time Clock/Timers

7.10.1. Overview

The Real Time Clock and Timer facilities on the BVME4500 are provided by the DP8570A Timer Clock Peripheral, which provides two 16-bit timer/counters, calendar/clock, a flexible interrupt scheme and 44 bytes of non-volatile RAM.

Two independent, multi-mode, 16 bit timers are provided. These timers operate in four modes. Each has its own pre-scaler and can select any of 8 possible clock sources. Thus, by programming the input clocks and the timer counter values a very wide range of time duration's can be achieved. The range is from 200nS (8MHz external clock) to 65,535 seconds (18hrs & 12min).

A very flexible and powerful on-chip interrupt structure is provided. Three basic types of interrupts are available: Periodic (from 1mS to 1 minute), Alarm/Compare (from the RTC) and Timer. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

For full programming details, refer to the DP8570A documentation detailed in the "Appendix A - Data Sheet & Manual References" section of this manual.

7.10.2. Hardware Specific Considerations

INTR pin Configuration

The INTR pin is fed to the Interrupt Controller (refer to "7.7. Interrupt Controller" for more details). It must be programmed as an active low, push-pull output. This is set up in the OUTPUT MODE REGISTER by programming bit 2 (INTR Active Hi/Low) CLEAR and bit 3 (INTR Push-pull/Open Drain) SET.

T1 pin Configuration

The T1 pin is not currently connected on the BVME4500.

MFO pin Configuration

The MFO pin is not currently connected on the BVME4500.

RTC Crystal Oscillator Frequency

The BVME4500 uses a 32.768 kHz crystal. This provides lowest power dissipation. The DP8570A needs to be programmed with the oscillator frequency used. This is set up in the REAL TIME MODE REGISTER by programming bits 7&6 (XT1 and XT0) both CLEAR.

TCK - External Timer Clock Input

TCK is driven from a fixed 8 MHz clock source.

PFAIL - Power Fail Input

This input is driven from the MAX791 power fail signal.

G0 & G1 - Timer Gate Inputs

These pins are pulled low on the BVME4500.

7.10.3. Programming

The register map of the DP8570A is shown below. The register map consists of two 31 byte pages with a main status register that is common to both pages. A control bit (bit 7) in the Main Status Register is used to select either page. Page 0 contains all the clock and timer functions, while page 1 has non-volatile RAM.

Page 0 is further sub-divided to provide two blocks of control registers. Again a bit in the Main Status Register (bit 6) is used to select either register block.

The registers are all byte wide mapped on the least significant byte of long word boundaries.

The registers must not be accessed for the first 64µS after reset.

Address	Page Select = 1	Page Select = 0	
		Register Select = 1	Register Select = 0
FF900003	Main Status Register		
FF900007	RAM	Real Time Mode	Timer 0 Control
FF90000B	RAM	Output Mode	Timer 1 Control
FF90000F	RAM	Interrupt Control 0	Periodic Flag
FF900013	RAM	Interrupt Control 1	Interrupt Routing
FF900017	RAM	$^1/_{100}$ Second Counter	
FF90001B	RAM	Seconds Clock Counter	
FF90001F	RAM	Minutes Clock Counter	
FF900023	RAM	Hours Clock Counter	
FF900027	RAM	Day of Month Clock Counter	
FF90002B	RAM	Months Clock Counter	
FF90002F	RAM	Years Clock Counter	
FF900033	RAM	Units Julian Clock Counter	
FF900037	RAM	100s Julian Clock Counter	
FF90003B	RAM	Day of Week Clock Counter	
FF90003F	RAM	Timer 0 LSB	
FF900043	RAM	Timer 0 MSB	
FF900047	RAM	Timer 1 LSB	
FF90004B	RAM	Timer 1 MSB	
FF90004F	RAM	Seconds Compare RAM	
FF900053	RAM	Minutes Compare RAM	
FF900057	RAM	Hours Compare RAM	
FF90005B	RAM	Day of Month Compare RAM	
FF90005F	RAM	Months Compare RAM	
FF900063	RAM	Day of Week Compare RAM	
FF900067	RAM	Seconds Time Save RAM	
FF90006B	RAM	Minutes Time Save RAM	
FF90006F	RAM	Hours Time Save RAM	
FF900073	RAM	Day of Month Time Save RAM	
FF900077	RAM	Months Time Save RAM	
FF90007B	RAM	RAM	
FF90007F	RAM	RAM/TEST	

7.11. EEPROM

The BVME4500 provides 2Kbits of EEPROM storage for configuration settings using an NM24C02 serial I^{2}C EEPROM device. The EEPROM I^{2}C bus is accessed via the following EEPROM registers. For full programming details, refer to the NM24C02 documentation detailed in the "Appendix A - Data Sheet & Manual References" section of this manual.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FFA0000F	EE-DIR	Reserved	Reserved	Reserved	Reserved	Reserved	SDA	Reserved	Reserved
FFA00027	EE-DAT	Reserved	Reserved	Reserved	Reserved	SCL	SDA	Reserved	Reserved

Bit 7-4: **Reserved.**
These bits are unused. When read, their state is undefined.

Bit 3: **SCL: Serial Clock Line.**
This is the I^{2}C Clock Line, used for clocking data in and out of the NM24C02 EEPROM. When the bit is SET in EE-DAT, the clock line is HIGH, when the bit is CLEAR in EE-DAT, the clock line is LOW.

Bit 2: **SDA: Serial Data Line.**
This is the I^{2}C Data Line, used for reading the data to/from the NM24C02 EEPROM. When the bit is SET in EE-DIR, the data will be OUTPUT to the EEPROM, when the bit is CLEAR in EE-DIR, data will be INPUT from the EEPROM. The EE-DAT register bit sets the data to the EEPROM in output mode, and reflects the data from the EEPROM in input mode.

Bit 1-0: **Reserved.**
These bits are unused. When read, their state is undefined.

7.12. Watchdog

The BVME4500 provides the software watchdog function available on the MAX791. The watchdog is accessed via two registers, one to enable the watchdog and one to toggle the watchdog.

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
FFA00013	WD-EN	Reserved	Reserved	Reserved	WDOG	Reserved	Reserved	Reserved	Reserved
FFA00033	WD-TG	Reserved	Reserved	Reserved	WDOG	Reserved	Reserved	Reserved	Reserved

Bit 7-5: **Reserved.**
These bits are unused. When read, their state is undefined.

Bit 4: **WDOG: WatchDog Enable/Refresh.**
This bit drives the input to the watchdog circuit. When the bit is CLEAR in WD-EN, the watchdog function is disabled. When the bit is SET in WD-EN, the watchdog is enabled and the bit must be toggled in WD-TG every second if a Watchdog time out is to be avoided. If the bit is not toggled in WD-TG within the time out period (1 second minimum) then a hardware reset will be generated.

Bit 3-0: **Reserved.**
These bits are unused. When read, their state is undefined.

7.13. Serial Communications Controller

7.13.1. Overview

The Serial Communications Controller (SCC) resource is based on the Z85230. This block provides two independent, full-duplex asynchronous serial communication channels. Each channel has its own baud rate generator, clocked from a variety of sources, including a Digital Phase Locked Loop (DPLL).

Each channel is independently electrically buffered as RS232 using MAX202E transceivers, which operate from a single +5V, removing the need of a +12V supply on the BVME4500 and offering ESD protection up to ±15kV. Connection is made via the front panel connectors (see “6.3. JP3A & JP3B Serial Port Connections”).

For full programming details, refer to the Z85230 documentation detailed in the "Appendix A - Data Sheet & Manual References" section of this manual.

7.13.2. Serial Clock Sources

PCLK This is the master Z85230 clock pin. It is used to synchronise all internal signals. It is available as a clock source to the baud rate generator. The BVME4500 drives this signal with the processor clock divided by 2. Thus with a 33MHz bus clock, the Z85230 is clocked at 16.5MHz. Because this pin is CPU clock dependent it is recommended that it is not used for baud rate generation.

RTxCA
RTxCB These input pins can be programmed to supply any combination of: the receive clock, the transmit clock, the baud rate generator and the DPLL. The BVME4500 drives these signals from an onboard 7.3728MHz.

TRxCA
TRxCB These pins are not connected on the BVME4500.

7.13.3. Programming

Each channel has a data register, when it is read, the receiver FIFO is read. When it is written, the transmitter FIFO is written.

Each channel also has a number of Write Registers and Read Registers that are used to control the operation of the channel. These are generally accessed as a two step procedure. First the register to be accessed is written to the Control Register, then the next access to the Control Register accesses the referenced Read or Write Register.

Address	Register Access
FFB00003	Control Register - Channel B (JP3B)
FFB00007	Data Register - Channel B (JP3B)
FFB0000B	Control Register - Channel A (JP3A)
FFB0000F	Data Register - Channel A (JP3A)

The BVME4500 supports vectored interrupts from the SCC, refer to "7.7. Interrupt Controller" for more details.

8. Specifications

8.1. On-Board Functions

MC68040 at 33MHz.

Z85230 Dual Serial interface controller, 7.3728MHz or CPU/2 clock source,
RS232 buffers, front panel connections.
DP8570A Timer Clock Peripheral (calendar-clock, 3 timers, 44 byte NVR).
85296CA DMA Ethernet Controller,
Front panel RJ-45 10baseT connection.
MAX791 Watchdog: refresh period = 1000mS (when enabled).

2Mbyte BOOTFLASH memory, 32-bit wide.
2Mbytes CMOS SRAM, 32-bit wide, battery backed (up to 3 years).
32-bit wide memory module interface with burst-fill up to 2/1/1/1.
2Kbit serial access EEPROM.
LOCAL BUS TIMEOUT period 64 CPU clocks (1.93µS).

RED LED indicates VMEbus MASTER access.
YELLOW LED indicates ETHERNET link.
GREEN LED indicates processor status.

RESET switch (if enabled).
ABORT switch (level 7 auto-vectored interrupt).

8.2. VMEbus Master

FAIR Bus Requester, single level.
A24, A16
D16, D08(EO)
RMW
AM6

8.3. VMEbus Slave

A24, A16
D16, D08(EO)
RMW
AM6
LOCATION MONITOR

8.4. VMEbus System Controller Functions

ARBITER: SGL, FAIR ROR (RWD option).
SYSCLK Driver.
SYSRESET Driver/Monitor power-up and switch.
VMEbus RESET minimum period = 200mS.
BUS TIMEOUT period 128µS.
BUS ERROR monitor.
ACFAIL monitor (level 7 auto-vectored interrupt).

8.5. VMEbus Interrupts

Interrupter D08(O) ROAK:
I(1-7) single level, software programmable;
Interrupt vector ID, software programmable.

Interrupt handler D08(O): I(1-7) all levels, software maskable.

8.6. Board Configuration

Configuration Switch/Links: 4-bit, software readable.

LINKS: ABORT/RESET switch enable;
VMEbus RESET IN/OUT enable;
VMEbus SYSTEM CONTROLLER functions;
CPU cache inhibit;
Ethernet I/F select.

PROGRAM: VMEbus SLAVE addressing;
VMEbus interrupt handler levels;
VMEbus interrupt level & vector ID;
Local SRAM & VMEbus mapping.

8.7. Operating Environment

Dimensions: 100mm x 160mm (3U) single slot.

Power: +5v 2.3A (max.), +12V 0mA, -12V 0mA.

Environmental: 0 to 70 °C, 95% humidity non-condensing (extended range to order).
Airflow across CPU heatsink (typical CPU dissipation):
0m/s @ 25 °C; 0.5m/s @ 50 °C; 2.0m/s @ 70 °C.

Appendix A - Data Sheet & Manual References

MC68040

MOTOROLA MC68040 MC68EC040 MC68LC040 MICROPROCESSORS USER'S MANUAL (1992, MOTOROLA order number: M68040UM/AD).

MOTOROLA PROGRAMMER'S REFERENCE MANUAL (1991, MOTOROLA order number: M68000PM/AD).

82596CA

INTEL 32-Bit Local Area Network (LAN) Compliant User's manual (1992, INTEL order number: 296853-001).

INTEL 82596CA HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR DATA SHEET (July 1992, INTEL order number: 290218-005).

DP8570A

NATIONAL SEMICONDUCTOR DP8570A Timer Counter Peripheral (TCP) Data Sheet (May 1993, TL/F/8638).

Z85230

ZILOG SCC User's Manual (Q4/1992).

AM29F800

AMD Flash Memory Products Data Book/Handbook 1996.

NMC24C02

NATIONAL SEMICONDUCTOR NMC24Cxx – Standard 2-Wire Bus Interface Serial EEPROM Family (May 1996).

MEM390 Memory Module

MEM390 4/8 Mbyte DRAM MEMORY MODULE User Manual (BVM part number: 454-68391).

MEM400 Memory Module

MEM400 16Mbytes DRAM 4/8 MBytes FLASH MEMORY MODULE User Manual (BVM part number: 454-61400).

MEM480 Memory Module

MEM480 16/32/48Mbytes DRAM MEMORY MODULE Installation Guide (BVM part number: 454-61480).

VMEbus

THE VMEbus SPECIFICATION (Sept 1987, VITA).

Appendix B - CPU Cache Coherency and Bus Snooping

The MC68040 is a third generation 68000 series processor with separate data and instruction caches of 4Kbytes each. The cache unit supports full copyback caching, in addition to write-through caching (as available on earlier processors), cache inhibited, and bus-serialised cache modes.

Copyback caching means that when data is written out by the program, it may only reach the cache, and not the main memory. This poses cache coherency problems over those normally associated with earlier 68000 series processors (e.g. 68030), as the main memory can contain stale data, affecting DMA operations transferring data from dual-ported memory as well as to dual ported memory.

Bus serialisation is required as the 68040's internal architecture has a high degree of parallelism. Reads and writes do not occur in the order in which they are defined by the programmer. Normally this causes no problem as the 68040 will detect any clashes and synchronise them, but if accesses are being made to I/O areas for example, the ordering of reads and writes are very important. Bus serialised regions cause correct ordering of the reads and writes.

It follows on from the above that it is important to be able to define regions of the address space as operating in different caching modes. This isn't strictly a caching issue, but is very relevant to the operation of system and user software.

Use is made of the 68040's "Transparent Translation Registers" and MMU "Page Tables" to define the caching mode for different regions of the address space.

The 68040's Transparent Translation Registers contain an address and mask field to allow definition of an address range to be used. They also contain fields to specify the relevant caching modes for the defined region. There are four registers, two for data DTT0 and DTT1 and two for instructions ITT0 and ITT1.

The TT0 registers override the TT1 registers if there is any overlap, and undefined regions will be accessed in the 68040's default mode (write-through caching enabled) if the MMU is disabled. If the MMU is enabled any regions undefined in the TT registers will be checked in the Page Tables. The Page Tables relate to a 4 or 8KByte region, and the caching mode is specified in a field of the page descriptor in a similar way to the TT registers.

With a 68040 processor, a cache-inhibited, bus-serialised region can be defined from $F0000000 to $FFFFFFFF for access to BOOTFLASH, SRAM, VMEbus A24, VMEbus A16 & on-board registers for supervisor access. The rest of the address space is defined as write-through caching for instructions and copy-back caching for data for supervisor mode. The page descriptors would be used to define the regions for user-state accesses, allocated on a dynamic basis (by operating system software). The values that need to be set into the 68040 TT registers to implement this scheme are as follows:

DTT0 = $F00FA040, DTT1 = $00FFA020, ITT0 = NOT USED, ITT1 = $00FFA000

Note that instruction caching only functions in write-through mode, not copy-back mode, as no writes occur to the instruction address space. To use write-through caching in place of copyback, the "$20" should be replaced by a "$00" in the above values for DTT1.

It is useful to have different regions defined for the same address space, because as the BVME4500 dual-maps some of the address space, it can be accessed in different caching modes. If the above scheme was adopted, then the VMEbus A24 space could be accessed at address $EE000000 as write-through cached, and at address $FE000000 as cache-inhibited bus-serialised access.

The BVME4500 has two separate blocks capable of bus mastership (DMA) other than the processor itself: the Ethernet Controller and the VMEbus Slave Interface. When any of these bus masters transfer data directly into a memory region (DMA), cache coherency problems can occur, as the processor may not know that data in it's internal caches is now invalid.

This problem can be approached in a number ways:

1. Normally main system memory resides on the BVME4500, and the 68040 can use "bus-snooping" to monitor accesses to the memory by any of the other bus masters. The bus-snooping must be enabled by programming the relevant bus-snoop enable bit(s) for the bus master in question. For the Ethernet Controller and VMEbus Slave Interface, there is a SNOOP ENABLE bit (refer to "7.8. VMEbus Slave Access Controller" for more details).

2. The 68040's internal caches can be "flushed" if it is known that their data may be invalid (e.g. when an interrupt occurs after a DMA operation). It may also be necessary to do a "cache push" if copyback caching is in use. This can be very wasteful, as data not involved in the transfers at all will also be purged from the caches.

3. Non-cached regions can be used to access the memory. For example, the Ethernet Controller can be set-up to DMA into a separate buffer region (e.g. the SRAM), which is accessed via a non-cached address. In this case, bus-snooping is not required, but the data, once DMAed into memory, is not subject to the advantages of caching. This does also have a potential performance advantage, as there is a timing overhead involved in bus-snooping by the 68040 processor.

Other schemes may be determined by the user, or a combination of the above may be used in conjunction.

Appendix C - Memory Module Pinout

M 1			M 2			M 3		
PIN	Name	Function	PIN	Name	Function	PIN	Name	Function
1	A31		1	/RST	Reset Module	1	D0	
2	A30		2	TT1	Transfer	2	D1	
3	A29		3	TT0	Type #	3	D2	
4	A28		4	TM2	Transfer	4	D3	
5	A27		5	TM1	Modifier#	5	D4	
6	A26		6	TM0		6	D5	
7	A25		7	+5V	5 Volt Power	7	D6	
8	A24		8	/WE	Write Enable #	8	D7	
9	A23	A	9	SIZ1	Transfer	9	D8	
10	A22	D	10	SIZ0	Size #	10	D9	D
11	A21	D	11	GND	Ground	11	D10	A
12	A20	R	12	/TS	Transfer Start #	12	D11	T
13	A19	E	13	/TIP	Trans. In Prog. #	13	D12	A
14	A18	S	14	/LOCK	Locked (RMW) #	14	D13	
15	A17	S	15	+5V	5 Volt Power	15	D14	L
16	A16		16	/TA	Transfer Ack. #	16	D15	I
17	A15	L	17	SC1	Snoop	17	D16	N
18	A14	I	18	SC0	Control #	18	D17	E
19	A13	N	19	GND	Ground	19	D18	S
20	A12	E	20	CLK	CPU Clock #	20	D19	
21	A11	S	21	GND	Ground	21	D20	#
22	A10		22	/MIRQ	Module IRQ	22	D21	
23	A9	#	23	/MI	Memory Inhibit #	23	D22	
24	A8		24	+5V	5 Volt Power	24	D23	
25	A7		25	GND	Ground	25	D24	
26	A6		26	CLK2	CPU Clock2 #	26	D25	
27	A5		27	GND	Ground	27	D26	
28	A4		28	MERR	Module Error	28	D27	
29	A3		29	N/C	No Connect	29	D28	
30	A2		30	GND	Ground	30	D29	
31	A1		31	+5VSB	5V Standby Power	31	D30	
32	A0		32	+12V	12 Volt Power	32	D31	

NOTES: This allows connection to a BVM Memory Module. # indicates a direct connection to the equivalent processor signal, see the MC68040 manual or data sheet for an explanation. /RST is a general reset signal, /MIRQ is an interrupt signal from the module, and MERR is a bus error signal from the module. The 12 volt power connection is not switched, and is intended for FLASH memory programming on those modules that support it. The 5 volt standby power supply is connected directly to the VMEbus +5STDBY line, and is intended for non-volatile SRAM backup on those modules that support it.

The interface is not intended for user connection, the pinout is provided here for reference only.

Some memory modules provide a JTAG programming strip to allow direct programming from the host module. This connector detail is known as M4, the connections are shown below, and are **for factory use only**.

M4			
PIN	Name	PIN	Name
1	TCK	6	Vcc
2	GND	7	TDO
3	TMS	8	GND
4	GND	9	TRST
5	TDI	10	ENABLE

Appendix D - Circuit Diagrams

Processor and Memory
863cd2_2.sch
2

This sheet contains:
Processor socket
SRAM
EPROM
MM Interface

Peripherals and Interrup
863cd5_2.sch
5

This sheet contains:
Serial Port
Real Time Clock
Peripheral Control PAL
Interrupt Control PAL

Ethernet
863cd3_2.sch
3

This sheet contains:
Ethernet Interface

- Takes CPUCLK1

Power and Reset
863cd6_2.sch
6

This sheet contains:
Reset Circuit
Oscillator Circuit
Battery Circuit
General De-Couplers

VME Interface
863cd4_2.sch
4

This sheet contains:
VMEI Interface
P1 Connectors

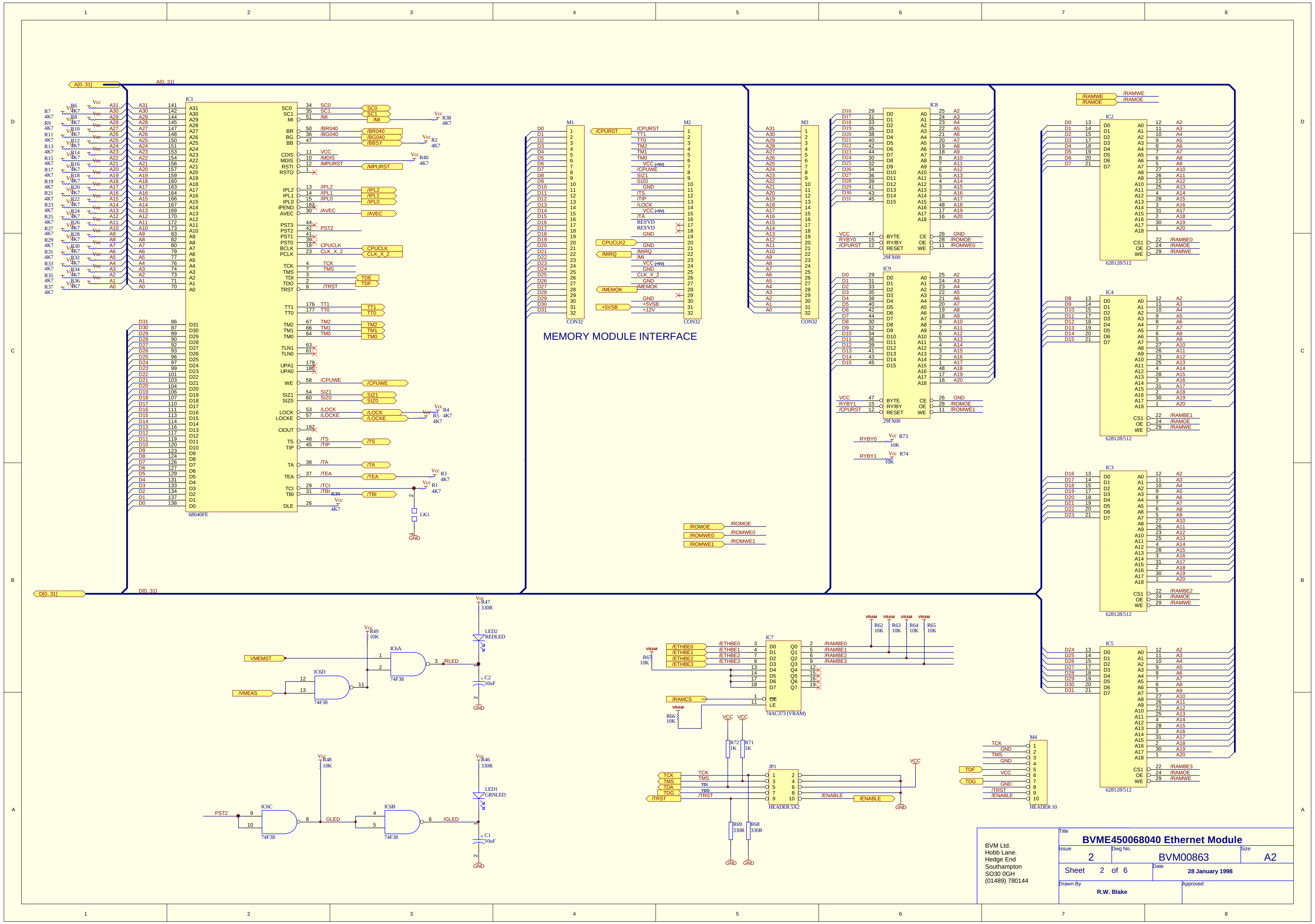
BVM Ltd.
Hobb Lane.
Hedge End
Southampton
SO30 0GH
(01489) 780144

Title
BVME4500 68040 Ethernet Module

Issue	Dwg No.	Size
2	BVM00863	A3

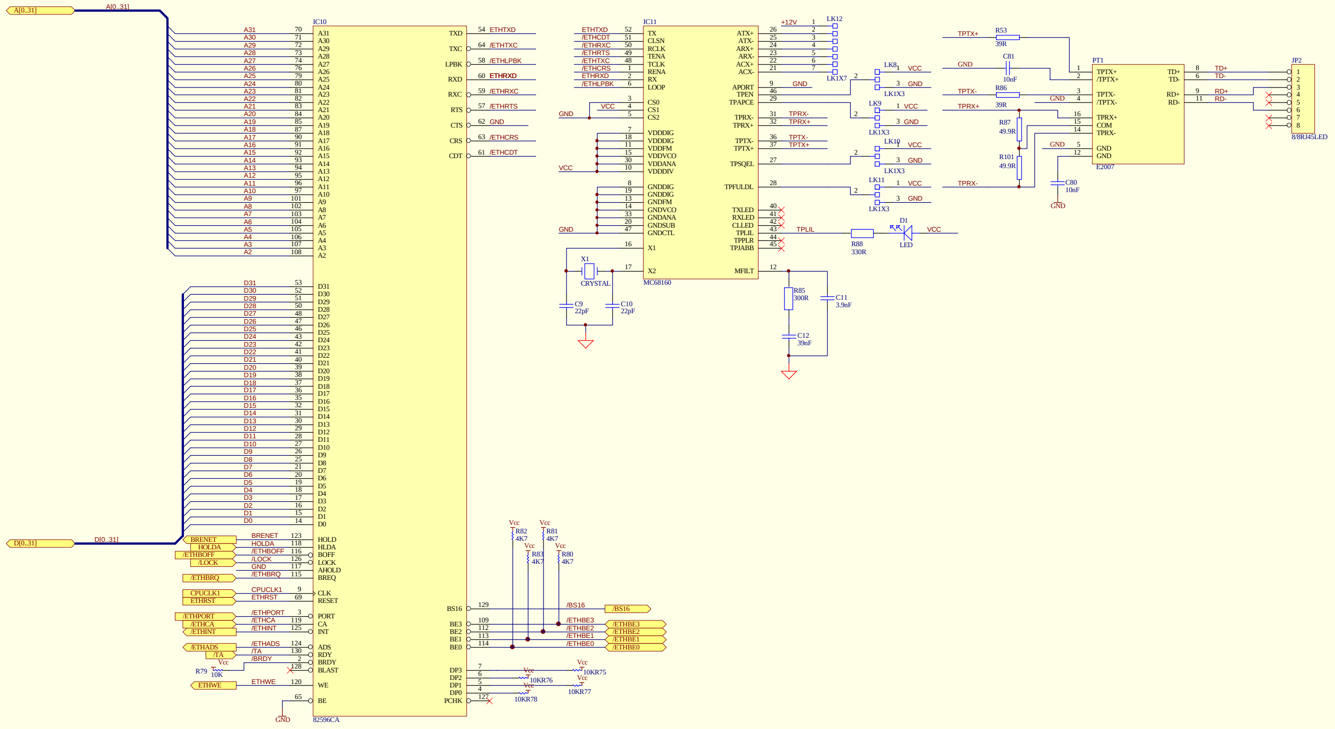
Sheet 1 of 6
Date **28 January 1998**

Drawn By **R W Blake**
Approved



BVM Ltd.
Hobb Lane.
Hedge End
Southampton
SO30 0GH
(01489) 780144

Title	BVME450068040 Ethernet Module	
Issue 2	Dwg No. BVM00863	Size A2
Sheet 2 of 6	Date 28 January 1998	
Drawn By R.W. Blake	Approved	



A[0..31]
D[0..31]
IC10
82596CA
A31 A30 A29 A28 A27 A26 A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2
D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
HOLD HLDA BOFF LOCK AHOLD BREQ CLK RESET PORT CA INT ADS RDY BRDY BLAST WE BE
TXD TXC LPBK RXD RXC RTS CTS CRS CDT
BS16 BE3 BE2 BE1 BE0 DP3 DP2 DP1 DP0 PCHK
ETHTXD /ETHTXC /ETHLPBK ETHRXD /ETHRXC /ETHRTS GND /ETHCRS /ETHCDT
BRENET HOLDA /ETHBOFF /LOCK /ETHBRQ CPUCLK1 ETHRST /ETHPORT /ETHCA /ETHINT /ETHADS /TA /BRDY ETHWE
/BS16 /ETHBE3 /ETHBE2 /ETHBE1 /ETHBE0
R79 10K
R82 4K7 R81 4K7 R83 4K7 R80 4K7
10KR75 10KR76 10KR77 10KR78
Vcc
IC11
MC68160
TX CLSN RCLK TENA TCLK RENA RX LOOP CS0 CS1 CS2
VDDDIG VDDDIG VDDFM VDDVCO VDDANA VDDDIV
GNDDIG GNDDIG GNDFM GNDVCO GNDANA GNDSUB GNDCTL
X1 X2
ATX+ ATX- ARX+ ARX- ACX+ ACX- APORT TPEN TPAPCE TPRX- TPRX+ TPTX- TPTX+ TPSQEL TPFULDL TXLED RXLED CLLED TPLIL TPPLR TPJABB MFILT
ETHTXD /ETHCDT /ETHRXC /ETHRTS /ETHTXC /ETHCRS ETHRXD /ETHLPBK
VCC GND +12V
X1 CRYSTAL
C9 22pF C10 22pF
R85 300R C11 3.9nF C12 39nF
LK12 LK1X7
LK8 LK9 LK10 LK11 LK1X3
TPLIL R88 330R D1 LED
TPTX+ TPTX- TPRX+ TPRX-
R53 39R C81 10nF R86 39R R87 49.9R R101 49.9R C80 10nF
PT1
E2007
TPTX+ /TPTX+ TPTX- /TPTX- TPRX+ COM TPRX- GND GND
TD+ TD- RD+ RD-
JP2
8/8RJ45LED

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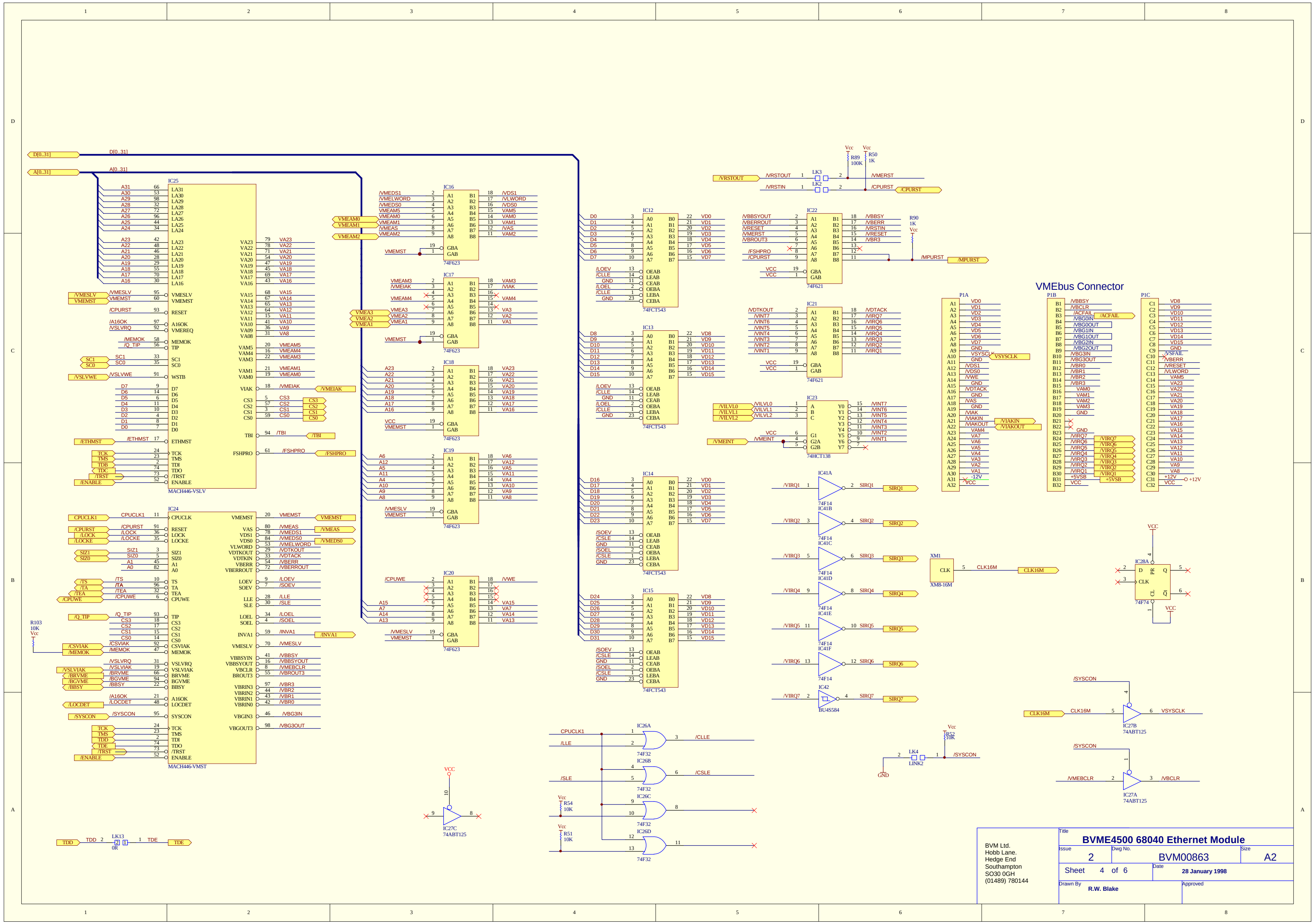
Title	BVME4500 68040 Ethernet Module		
Issue 2	Dwg No. BVM00863		Size A2
Sheet 3 of 6		Date 28 January 1998	
Drawn By R.W. Blake		Approved	



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Title **BVME4500 68040 Ethernet Module**

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Sheet 4 of 6 Date **28 January 1998**

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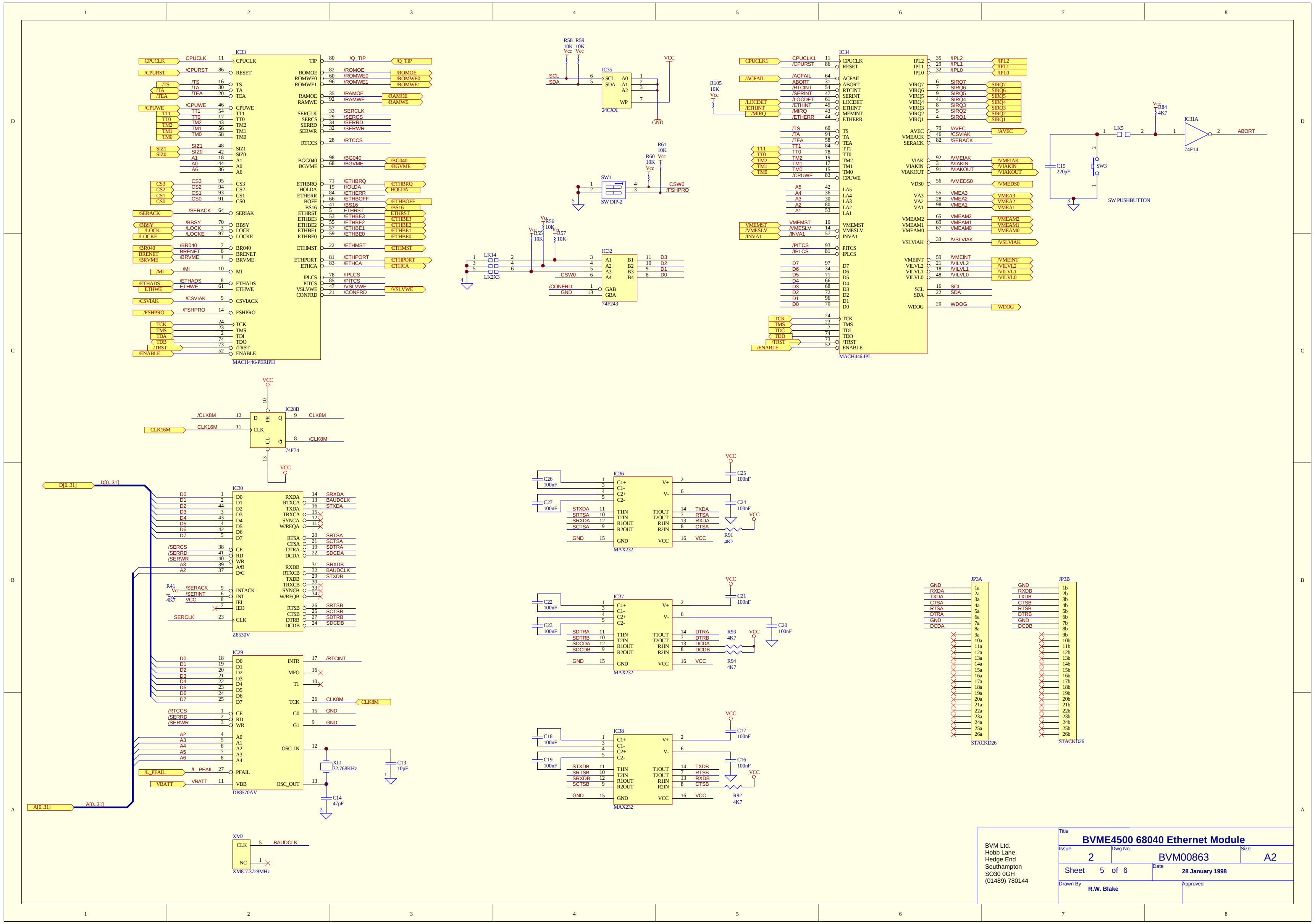

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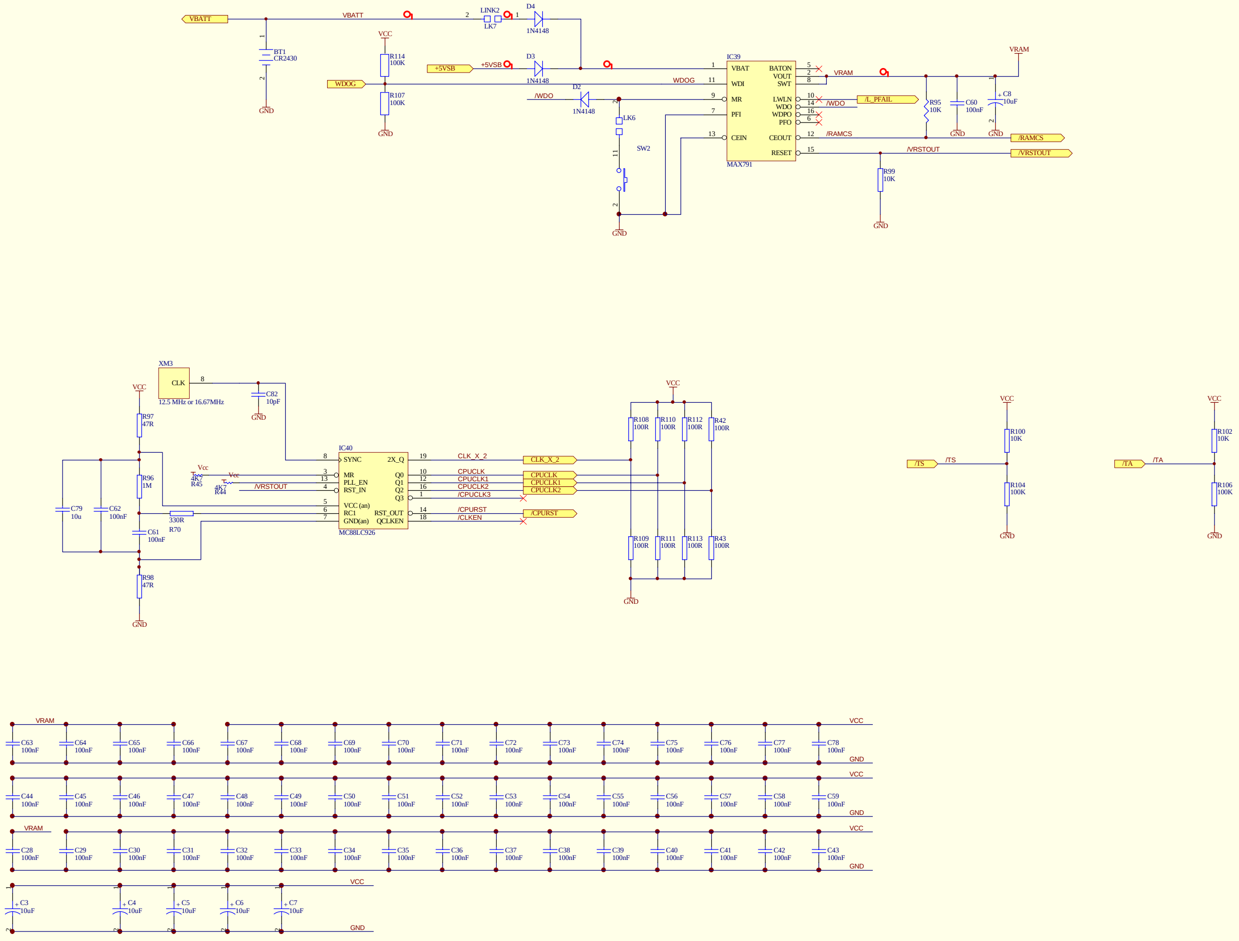

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